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TECHNICAL REPORT

colour inside

Photonic integrated circuits –
Part 1: Introduction and roadmap for standardization

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Part 1: Introduction and roadmap for standardization

FOREWORD

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IEC TR 62072-1, which is a Technical Report, has been prepared by subcommittee 86C: Fibre optic systems and active devices, of IEC technical committee 86: Fibre optics.

The text of this Technical Report is based on the following documents:

Enquiry draft	Report on voting
86C/1428/DTR	86C/1441/RVDTR

Full information on the voting for the approval of this technical report can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 63072-1 series, published under the general title *Photonic integrated circuits*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

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PHOTONIC INTEGRATED CIRCUITS –

Part 1: Introduction and roadmap for standardization

1 Scope

This part of IEC 63072, which is a Technical Report, provides an introduction to photonic integrated circuits (PICs) and describes a roadmap for the standardization of PIC technology over the next decade.

NOTE The trademarks and trade names mentioned in this document are given for the convenience of users of this document; this does not constitute an endorsement by IEC of these companies.

2 Normative references

There are no normative references in this document.

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
photonic integrated circuit
PIC
integrated circuit that contains optical structures to guide and process optical signals

3.2
III-V
three-five
compound semiconductor formed of materials from the third and fifth column of the periodic table

EXAMPLE 1 Indium phosphide

EXAMPLE 2 Gallium arsenide

3.3
through-silicon-via
TSV
metallised hole (via) through a silicon wafer enabling electrical conductivity from one surface of the silicon to the other

3.4
silicon photonics
structure or system of structures fabricated into a silicon wafer to guide light and enable passive and active optical processes to be carried out at the integrated circuit level

3.5
silicon-on-insulator
SOI
structure or system of structures fabricated into a silicon wafer to guide light and enable passive and active optical processes to be carried out at the integrated circuit level

3.6
vertical cavity surface emitting laser
VCSEL
semiconductor laser diode with direction of laser emission perpendicular to top surface

3.7
Mach-Zehnder interferometer
MZI
waveguide structure whereby an incident optical signal is split into two paths and allowed to recombine into an output signal and on which the phase variance between the two recombined signals can be manipulated to allow modulation of the output signal or switching between two or more input and output signals

3.8
ring resonator
closed optical path in which the optical radiation circulates in an optical loop in the same direction

Note 1 to entry: Standing waves are possible to exist at particular wavelengths.

3.9
micro-ring resonator
MRR
closed ring resonator waveguide structure on a PIC

Note 1 to entry: When located near a waveguide, the MRR will selectively couple out of the waveguide optical radiation only at the wavelengths λ_m, which satisfy the following resonance condition: MRR optical path length = $2\pi n_{eff} = m\,\lambda_m$, where n_{eff} is the effective refractive index of the MRR waveguide and m is a positive integer.

3.10
resonator finesse
F
quantity describing the sharpness of a resonant peak relative to the free spectral range of the resonator, obtained by dividing free spectral range (FSR) of a resonator by full width half maximum (FWHM) of a resonant peak

3.11
quality factor of a ring resonator
resonator finesse multiplied by the mode number m, where $m = 2\pi n_{eff/}\,\lambda_m$ and where n_{eff} is the effective refractive index of the ring resonator and λ_m is the resonant wavelength

3.12
large-scale integration
LSI
process of integrating thousands of transistors onto a single semiconductor chip

3.13
buried oxide
BOX
silicon dioxide (SiO_2) layer buried in silicon wafers to form silicon-on-insulator assemblies

Note 1 to entry: BOX layer is typically buried at less than 100 nm to several micrometers beneath the wafer surface depending on application. BOX layer thickness typically ranges from 40 nm to 100 nm.

3.14
grating coupler
GC
periodic grating structure on the surface of a PIC, which redirects light propagating in a waveguide in the PIC out through the surface of the PIC, typically at a small angle normal to the PIC surface

Note 1 to entry: This is the preferred method of coupling light into and from a PIC and typically uses a single-mode fibre or single-mode fibre array with an 8° angled interface. Therefore grating couplers are usually designed to redirect light into and out of the PIC at an angle of 8° normal to the PIC surface.

3.15
single polarization grating coupler
SPGC
grating coupler designed to couple light of one linear polarization to and from a waveguide in the PIC

3.16
polarization splitting grating coupler
PSGC
grating coupler designed to split the light incident on the PIC into two orthogonal linear polarizations, which are conveyed along two separate corresponding waveguides in the PIC

3.17
laser induced forward transfer
LIFT
direct-writing technique allowing the deposition of tiny amounts of material from a donor thin film through the action of a pulsed laser beam

3.18
complementary metal oxide semiconductor
CMOS
technology for constructing low power integrated circuits typically used in microprocessors, microcontrollers, static RAM, and other digital logic circuits

3.19
high speed phase modulator
HSPM
device allowing the phase of an optical signal to be rapidly varied

Note 1 to entry: One example of a HSPM is a PN junction on one of the waveguide branches of a MZI in a PIC, which causes a change in refractive index in response to the density in charge carriers passed through it.

4 Photonic integrated circuit (PIC)

4.1 Overview

A PIC is an integrated circuit on which operations can be carried out on light conveyed through it. One could think of a PIC as a miniature optical train, i.e. a sequence or collection of elements or structures, which perform an operation on one or more incident light beams. These operations may include modulation, wavelength dependent and independent switching, wavelength multiplexing/demultiplexing, power splitting, filtering, amplification, light generation (lasers) and light detection (detectors). Depending on the available chip size, element size and layout efficiency of optical elements and structures, a PIC can incorporate functions of varying complexity.

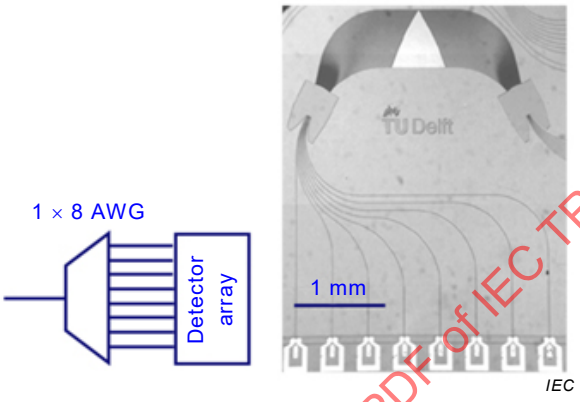
PICs operate on information signals imposed on optical wavelengths typically within the infrared 850 nm to 1 650 nm portions of the electro-magnetic spectrum reserved for fibre optic communication.

PICs can accommodate huge bandwidth densities, for example high data rates of information conveyed along tiny channels, which can be very densely arranged at the chip level. For this reason, PIC products are primarily deployed in the optical fibre communications market.

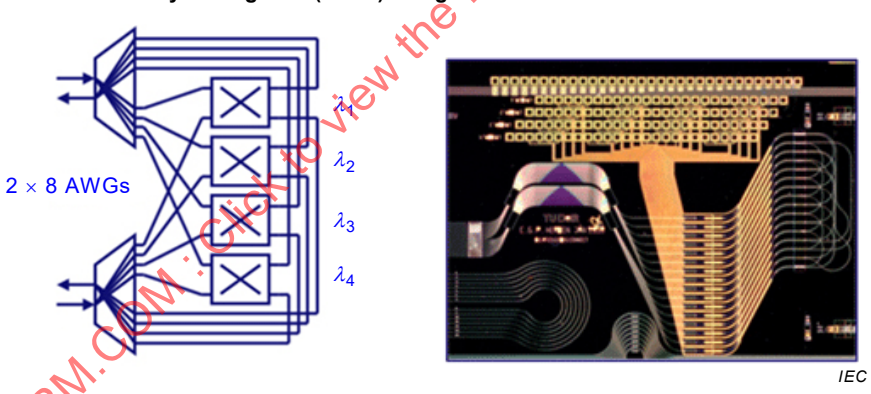
Optical sensors, however, represent a promising emerging application field for PICs, in which they can be used in the medical, aerospace, energy, automotive and defence sectors.

PICs are also widely anticipated to play a key role in the future commercialisation of quantum computers.

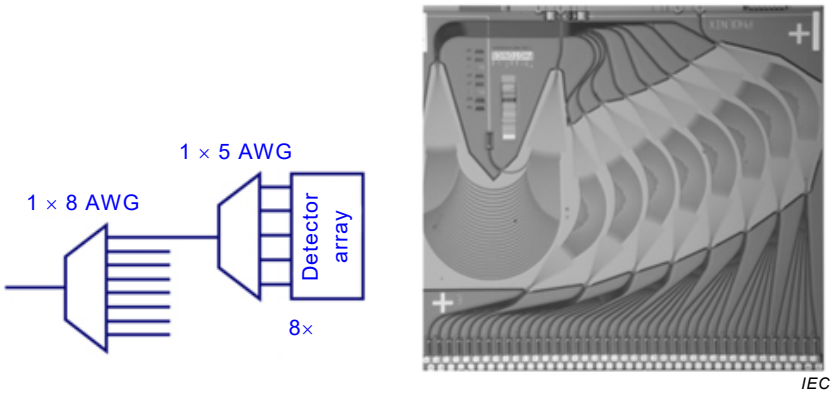
Figure 1 shows some examples of PICs of varying complexity and functionality.



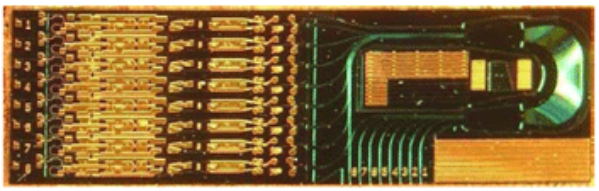
a) Wavelength-division multiplexing (WDM) receiver consisting of an array waveguide (AWG) integrated with an 8 detector diode



b) 4-channel 2 × 2 WDM cross-connect integrating 2 AWGs with 16 Mach-Zehnder interferometer switches in dilated configuration (66 components in total)



c) 40-channel WDM monitor chip integrating 9 AWGs and 40 detector diodes



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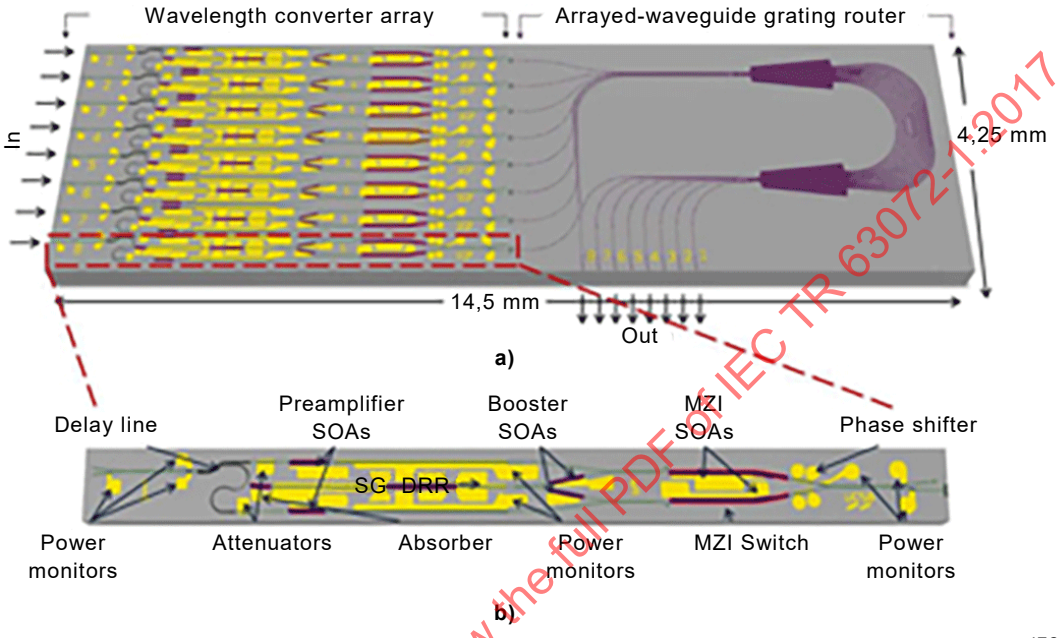
d) 8 × 8 channel wavelength router, integrating 8 wavelength converter circuits with an 8 × 8 AWG, with over 175 components



e) Detail of wavelength converter section

SOURCE Institute of Physics

Figure 1 – Examples of PICs [1][1]

4.2 PIC families

4.2.1 General

The fabrication techniques for PICs are similar to those used in electronic integrated circuits, in which photolithography is used to pattern semiconductor wafers for etching and material deposition.

Unlike electronic integration where silicon is the dominant material, PICs can be fabricated from a variety of semiconductor materials including silicon, indium phosphide (InP) and gallium arsenide (GaAs), and different material systems, including electro-optic crystals such as lithium niobate, silica-on-silicon and silicon-on-insulator (SOI).

Different materials provide different advantages and limitations depending on the functions to be carried out.

1 Figures in square brackets refer to the Bibliography.

4.2.2 Silicon photonics

Silicon PICs enable direct co-integration of the photonics with transistor based electronics; however, as an indirect bandgap material, silicon PICs will typically require separate elements for light generation and detection. Although it was shown in 2005 that silicon can be used to generate laser light via the Raman effect, such lasers would need to be optically driven rather than electrically driven, which would require an additional optical pump laser source [2].

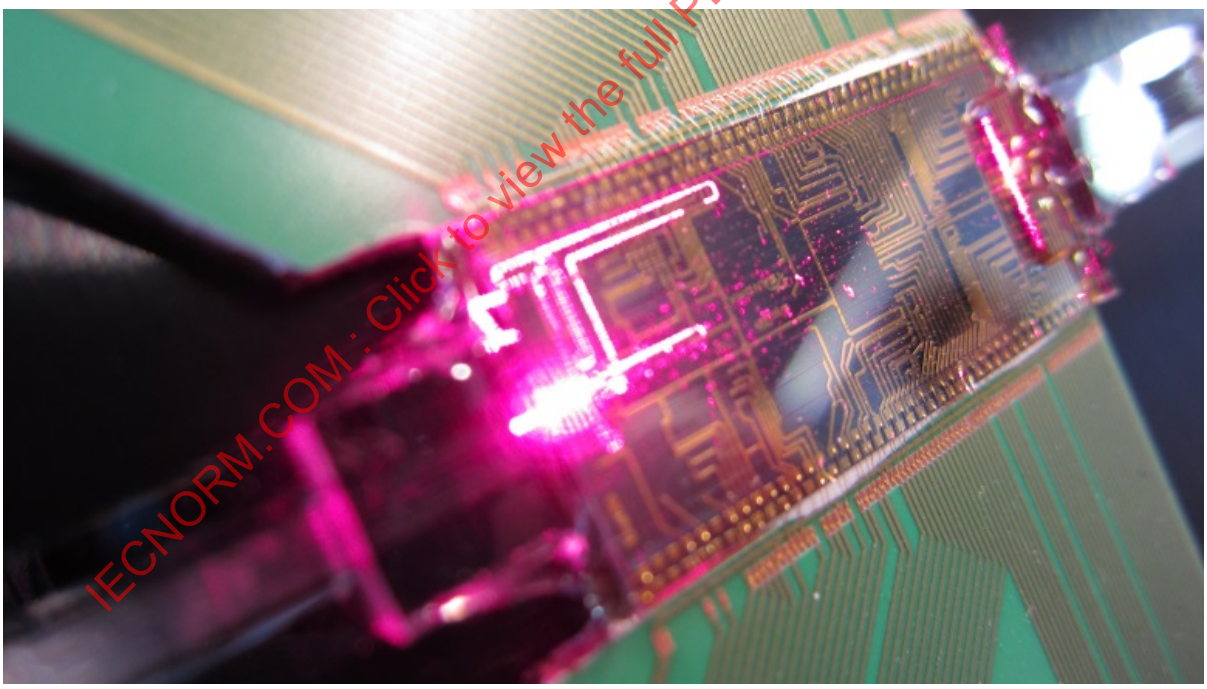
4.2.3 III-V photonics

PICs based on so called direct bandgap materials, such as indium phosphide or gallium arsenide, do allow the direct integration of light sources and detectors on the same integrated circuit; however, the foundry infrastructure is much more limited when compared to silicon wafers, leading to III-V PICs being typically restricted to low volume, high cost applications.

4.2.4 Silica and silicon nitride PICs

Silica (silicon dioxide) based PICs have very desirable properties for passive photonic circuits such as arrayed waveguide gratings (AWGs) due to their comparatively low losses and low thermal sensitivity.

Silicon nitride (Si_3N_4) based PICs are also becoming a leading material candidate for PICs in the datacom space, mainly due to the lower optical losses introduced and the inherent complementary metal oxide semiconductor (CMOS) compatibility with the electronics fabrication processes (see Figure 2).



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SOURCE Photo courtesy of SATRAX B.V., www.satrax.nl

Figure 2 – Optical beam forming network fabricated in TriPleX (silicon nitride)

Currently, the two most commercially utilised material platforms for PICs are based on silicon and indium phosphide.

4.3 Manufacturing capabilities

As of 2016, there were only a handful of organisations that could directly manufacture PICs. These included STMicroelectronics (France-Italy), Intel (US), and AMS (Austria).

Given the long turn-around for PIC wafer fabrication, the concept of multi project wafers was introduced by which a variety of different PIC designs from different organisations (usually small to medium enterprises) could be incorporated onto a single wafer, allowing a variety of different designs to be fabricated at once. Access to PIC fabrication by small to medium enterprises has been made possible through so-called multi-project wafer platforms, including JEPPIX (http://www.jeppix.eu/) for III-V photonics, EPIXFAB (http://www.epixfab.eu/) for silicon photonics, and TRIPLEX ("http://www.lionixbv.nl/triplex-integrated-optics) for silicon nitride photonics.

4.4 Global market

As of 2013, North America was the leader in the PIC market with 49 % market share; however, it is estimated that Asia-Pacific (APAC) will emerge as the market leader by 2022, growing at a compound annual growth rate (CAGR) of 35,9 % from 2012 to 2022.

The PIC market is expected to yield revenue growth from $150,4 million in 2012 to $1 547,6 million by 2022, at an estimated CAGR of 26,3 % from 2012 to 2022 [3].

As of 2015, some of the leading global organisations selling PIC products are Infinera Corporation (USA), NeoPhotonics Corporation (USA), Luxtera (USA), Mellanox (Israel) and OneChip Photonics (Canada).

4.5 Global government investment in PIC research and development

4.5.1 General

In addition to large scale research and development on PIC technologies, as of 2016, there has been renewed global government level investment into PIC development, which is seen as a key enabling technology.

4.5.2 United States of America

The importance of developing an integrated photonic eco-system was underscored by the launch in 2016 of the American Institute of Manufacturing Integrated Photonics (AIM), a public-private partnership providing over $610m worth of funding (http://www.aimphotonics.com/).

4.5.3 Europe

As of 2016, the European Commission Horizon2020 framework programme has provided and was expected to continue to provide substantial funding towards integrated photonics technologies between 2014 and 2020 of a similar order to that of the United States AIM initiative.

4.5.4 Japan

Photonics Electronics Technology Research Association (PETRA) is an incorporated technology research association, established on August 24, 2009. The organization is approved by METI (Ministry of Economy, Trade and Industry) under the Japanese Act on an Incorporated Research and Development Partnership. PETRA carries on national research and developments projects on leading-edge photonics and electronics converged devices and systems in the information and communication technology area, where photonics technology and electronics technology are mutually incorporated.

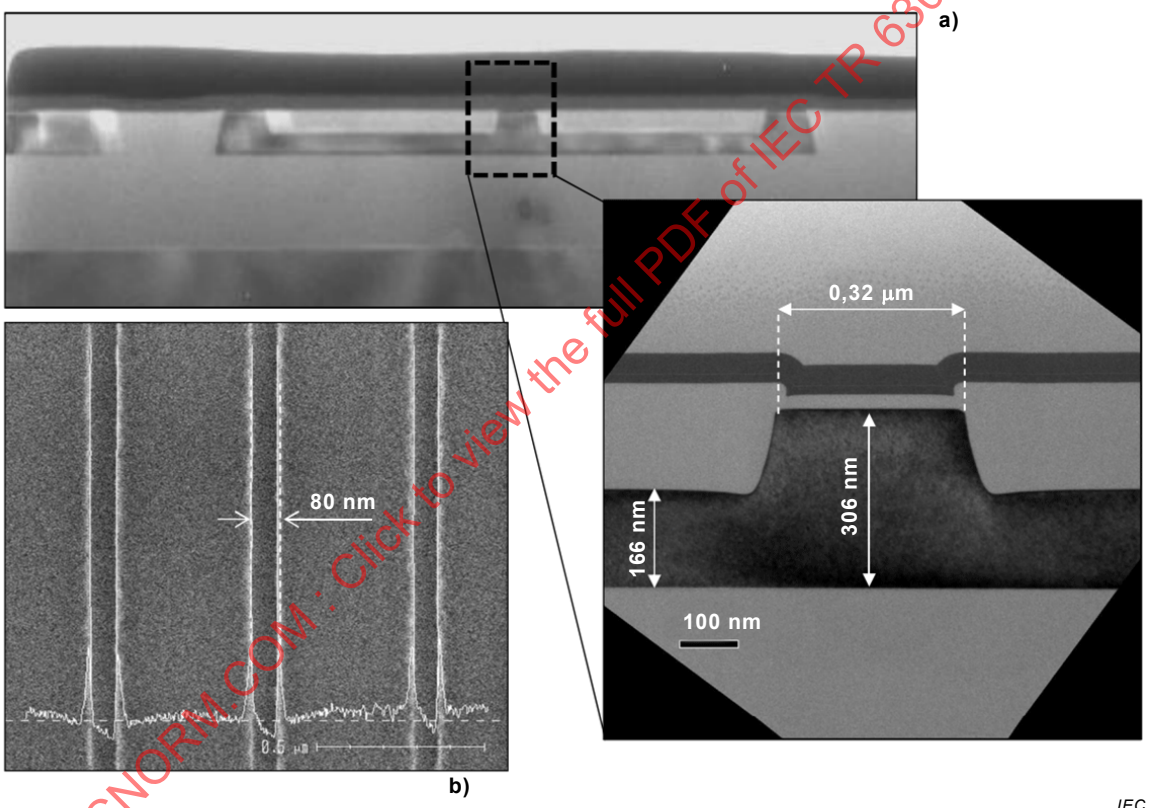
5 Silicon photonics

5.1 Overview

Silicon photonics is the study and application of PICs, which use silicon as an optical medium and offers the promise of high volume, low cost PIC fabrication in the near future, as it leverages currently available CMOS manufacturing infrastructures. This allows silicon PICs to be manufactured using existing semiconductor fabrication techniques.

The silicon-on-insulator (SOI) configuration, whereby a layer of silicon is bounded by a layer of silica, is the preferred choice for passive PIC structures, including multi-mode interference (MMI) structures, directional couplers, mode converters, in-plane couplers, out-of-plane (angled or vertical) grating couplers, splitters, optical filters polarization rotators and polarization beam splitter/combiners [4], [5].

Figure 3 shows an example of single-mode silicon waveguides fabricated on SOI substrates.



SOURCE IEEE

Key

(a) λ = 1,31 µm single mode waveguide cross-section

(b) Top view scanning electron microscope image of semi-dense 80 nm trenches

Figure 3 – Typical silicon waveguides [6]

5.2 Integration schemes

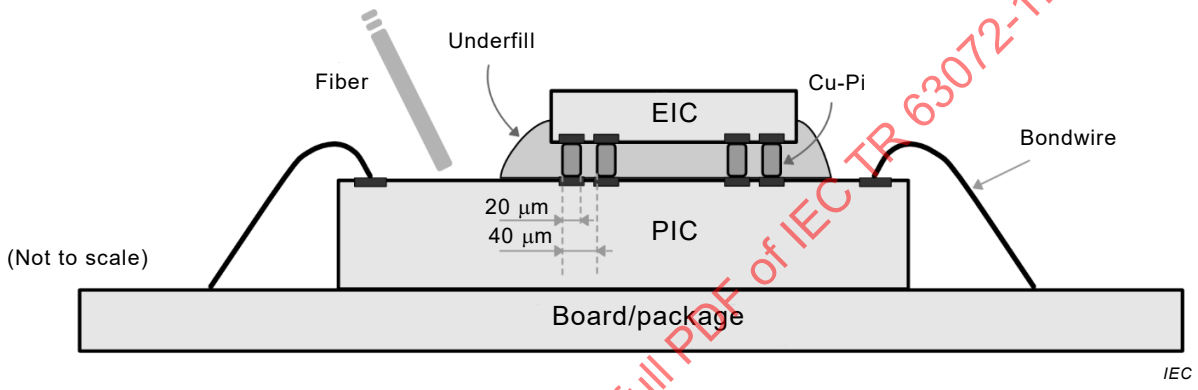
5.2.1 General

Integration of optical and electronic functionality on a PIC can be achieved through either heterogeneous integration, where separate optical and electronic chips are assembled onto each other [7], or by homogenous integration [8], [9], where optical and electronic circuits are built on the same chip [10].

5.2.2 Heterogeneous integration

As silicon is also the substrate used for most electronic integrated circuits (EICs), heterogeneous (or hybrid) integration of separate EICs and PICs provides a lower risk pathway to developing "active" PICs that combine complex electronic functionalities such as transimpedance amplifiers and modulators with photonic structures and elements.

The main advantage of heterogeneous integration is that the EICs and PICs are separately fabricated to achieve their respective optimised performances before bringing both elements together [11], while with homogenous fabrication, there is an inherent compromise on fabrication and performance. The disadvantage of heterogeneous integration is, however, a more complicated packaging and assembly process, limited density, more power dissipation and worse RF performance. An example of heterogeneous (or hybrid) integration based on flip-chip connection through copper pillars is shown in Figure 4.



SOURCE University of Pavia

Figure 4 – Heterogeneous integration by flip chip and copper pillars

5.2.3 Homogenous integration

Homogenous (or monolithic) integration allows packaging and assembly to be simplified, as now electronic and optical circuits are co-fabricated on the same chip. Homogenously integrated solutions typically rely either on SOI wafers [9], [11], [12], or on bulk silicon [8].

5.3 Non-linear behaviour

The propagation of light through silicon devices is governed by a range of nonlinear optical phenomena including the Kerr effect, the Raman effect, two photon absorption, and interactions between photons and free charge carriers. The presence of nonlinearity is of fundamental importance, as it enables light to interact with light, thus permitting applications such as wavelength conversion and all-optical signal routing in addition to the passive transmission of light.

6 III-V photonics

6.1 Indium phosphide (InP) photonics

Unlike silicon, indium phosphide (InP) is a direct bandgap material and thus allows for the co-integration of various optically active and passive functions on the same chip, including optical sources, amplifiers (gain elements), waveguides, modulators, and receivers.

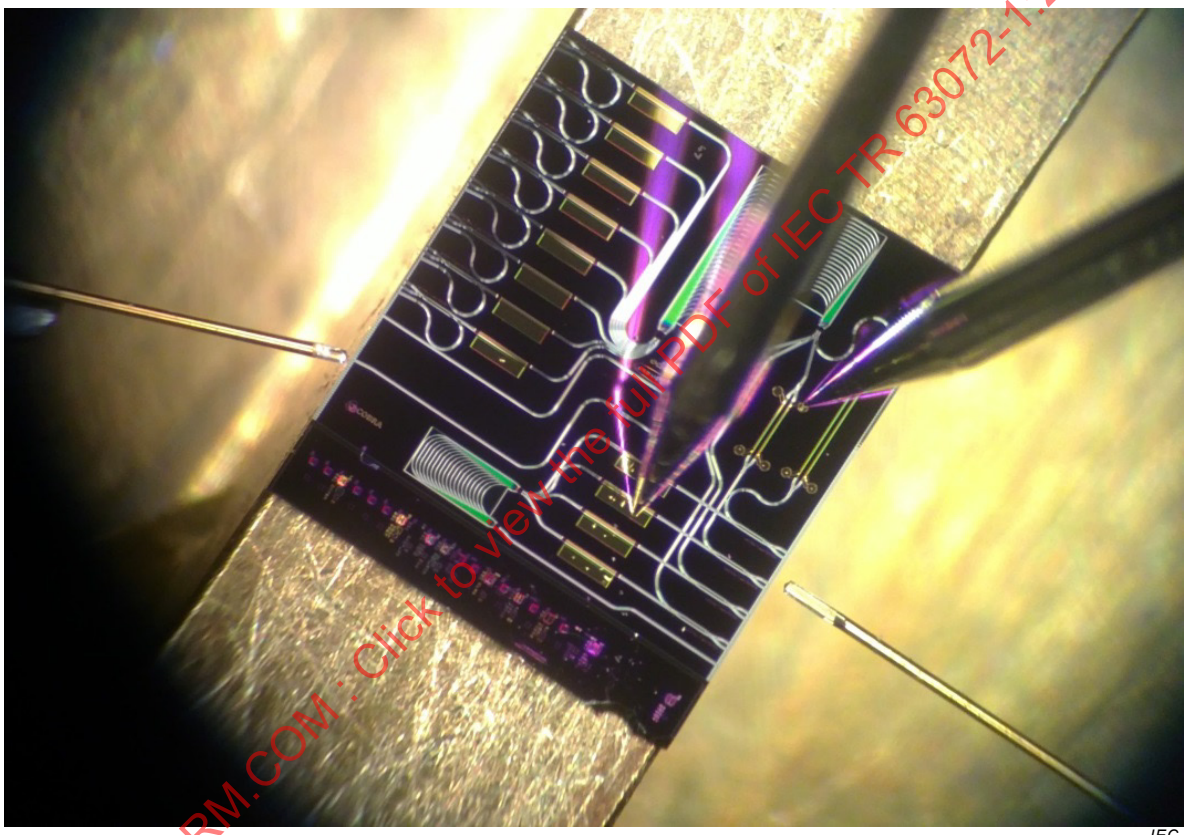
Early examples of InP PICs were distributed Bragg reflector (DBR) lasers, consisting of two independently controlled elements, namely a gain chip and a DBR mirror section.

Most modern monolithic tuneable lasers, externally modulated lasers (EMLs), and integrated receivers are based on InP PICs.

The most notable global academic centres of excellence for InP PIC research are the University of California at Santa Barbara, USA, and the Technology University of Eindhoven in the Netherlands.

Although III-V based photonics is widely accepted as the most mature integration technology due to its capability to deliver high-performance active devices, it still remains inherently a low volume, high margin technology due to the relatively low availability III-V wafer foundries when compared to CMOS infrastructures and processes.

Figure 5 and Figure 6 are examples of indium phosphide PICs.



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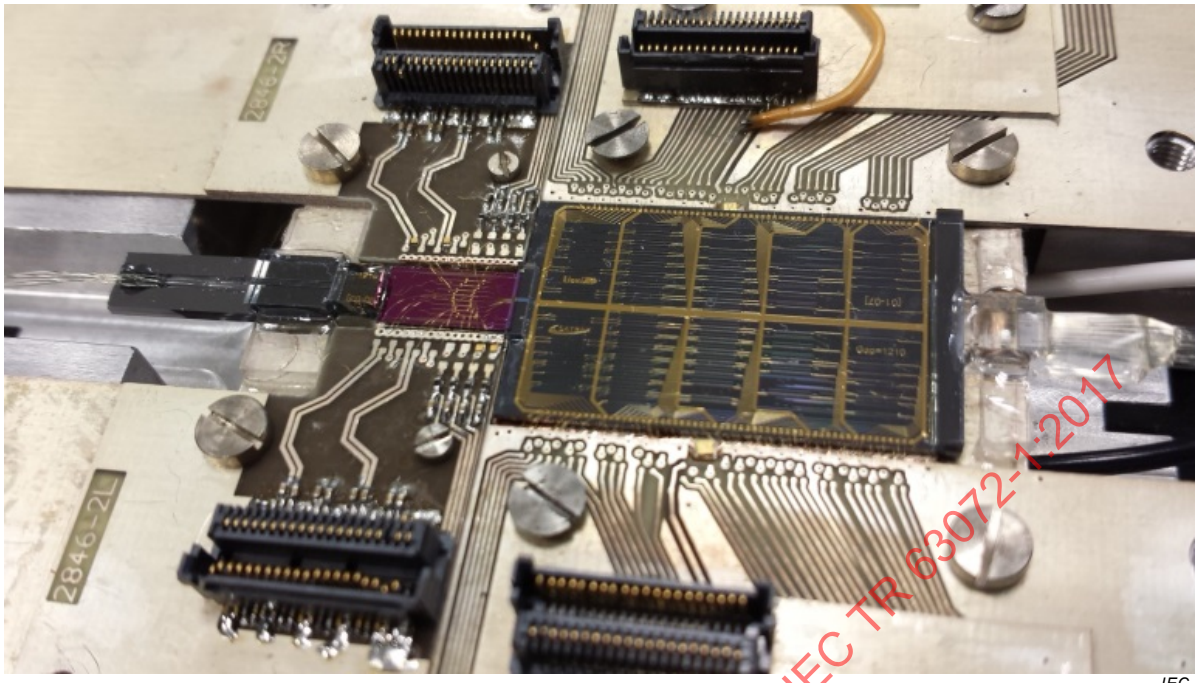
SOURCE Heinrich Hertz Institute

Figure 5 – Indium phosphide PIC with many structures, including AWG



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SOURCE Photo courtesy of SATRAX B.V., www.satrax.nl

Figure 6 – Combined InP and TriPleX microwave photonic beam-forming network

7 PIC transceiver – A simple example

7.1 Overview

One of the simplest PIC functions is a transceiver PIC, which, on the transmitter section of the PIC, takes continuous wave light from an optical source (either monolithically integrated, heterogeneously assembled or external) and passes it along a waveguide to a modulator, which is typically driven by an electronic signal through a variety of possible modulation mechanisms described below. The modulated light is then further conveyed along an integrated waveguide to an external coupler, which couples the light out of the PIC, typically to a single-mode optical fibre. On the receiver section of the transceiver PIC, modulated light received by the PIC through an external coupler, is conveyed to a detector (either monolithically integrated, heterogeneously assembled or external), which, through appropriate circuitry (typically a trans-impedance amplifier and limiting amplifier), converts the output of the detector into a corresponding electronic signal.

Figure 7 shows a schematic view of a four channel PIC transceiver, which operates as described in 7.2 and 7.3.

7.2 Transmitter section

First, a laser diode is powered to provide a source of continuous wave light. In this example, the laser is a separate device, which is attached to the PIC, though often the laser source is located remotely and conveys continuous wave (CW) light to the PIC via a fibre.

The CW laser light is coupled into the PIC through a single polarization grating coupler (SPGC) and the power is split equally across four waveguides. In each of the four waveguides, the CW light is conveyed through a Mach-Zehnder interferometer (MZI) with high speed phase modulators (HSPM) devices arranged in a "push-pull" configuration on each MZI waveguide branch. The HSPM pair is driven by a differential electrical signalling voltage conveyed via the small form factor pluggable (SFP) compliant high speed electrical interface. The application of voltage difference on each HSPM gives rise to a corresponding change in refractive index

along the section of the MZI waveguide branch over which the HSPM operates. This in turn causes opposite shifts in the phases of CW light passing in each waveguide branch. Upon merging of the MZI waveguide branches, the two light signals recombine to either interfere constructively, whereby the CW light leaves the MZI, or destructively whereby no light leaves the MZI. This effectively gives rise to a modulated optical output driven by the differential electrical signal.

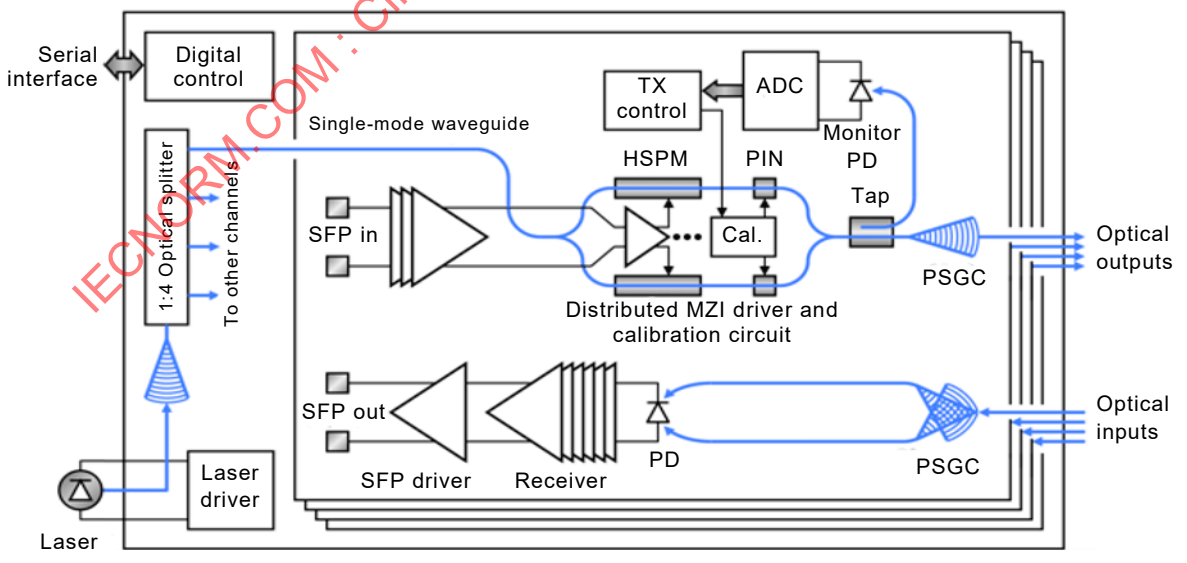
The waveguide leaving the MZI leads to a single polarization grating coupler (SPGC), which deflects the single polarization of light out of the waveguide and typically into an external single-mode fibre.

A small fraction of the light leaving the MZI is coupled into a tap waveguide, which is then conveyed to a monitor photodiode (PD). This is conveyed across an analogue-to-digital converter circuit to a calibration circuit on the MZI. The calibration circuit controls the current passing across two PIN junctions subtending a section of each MZI waveguide branch. Each PIN junction can be used to change the refractive index of the waveguide section it subtends by altering the charge density across it, thus it provides an additional means of tuning the phase of light in each branch and is used to calibrate the MZI.

7.3 Receiver section

Modulated light is conveyed from an external conduit, typically a single-mode optical fibre, into a polarization splitting grating coupler (PSGC), which decomposes the incident light into two orthogonal polarizations and conveys each polarization component along a separate waveguide. PIC waveguides are polarization sensitive, but the use of the PSGC means that the incident fibre need not be arranged so that all light is conveyed in one polarization axis and the incident fibre need not be adjusted so that said polarization axis matches the corresponding polarization axis of the PIC waveguide, which would be prohibitive in practise.

The optical path lengths of the two waveguides are matched and they converge on a photodiode, which in turn converts the received light into a corresponding electrical current. The current is passed through a receiver circuit, typically comprising a trans-impedance amplifier, which converts the current into a differential voltage. The differential voltage is then passed out through an electrical high speed signalling interface.



SOURCE: IEEE

Figure 7 – Schematic of four channel PIC transceiver by Luxtera [6]

8 Optical sources

8.1 Overview

Whatever the function of the PIC, optical sources (monolithically integrated, heterogeneously assembled or external) are a prerequisite to operation, and thus the optical communications industry has placed great importance in the fabrication and assembly of sources.

8.2 Advances in III-V integration onto silicon PICs

Integrated laser sources rely almost exclusively on III-V materials (InP, GaAs) in their active region, while silicon, as an indirect bandgap material, cannot serve as a practical laser source. Thus the preferred means of conveying light onto silicon PICs is through the use of separate III-V sources, which are either used as discrete external sources, from which light is conveyed through a passive optical coupling element on to the silicon PIC, or through heterogeneous assembly of III-V sources onto the silicon PIC chip.

The epitaxial growth of III-V material onto silicon is, however, made challenging by the inherent mismatch in lattice and thermal coefficients between the III-V and the silicon materials, which has led to poor performance and reliability in early attempts at heterogeneous integration [13].

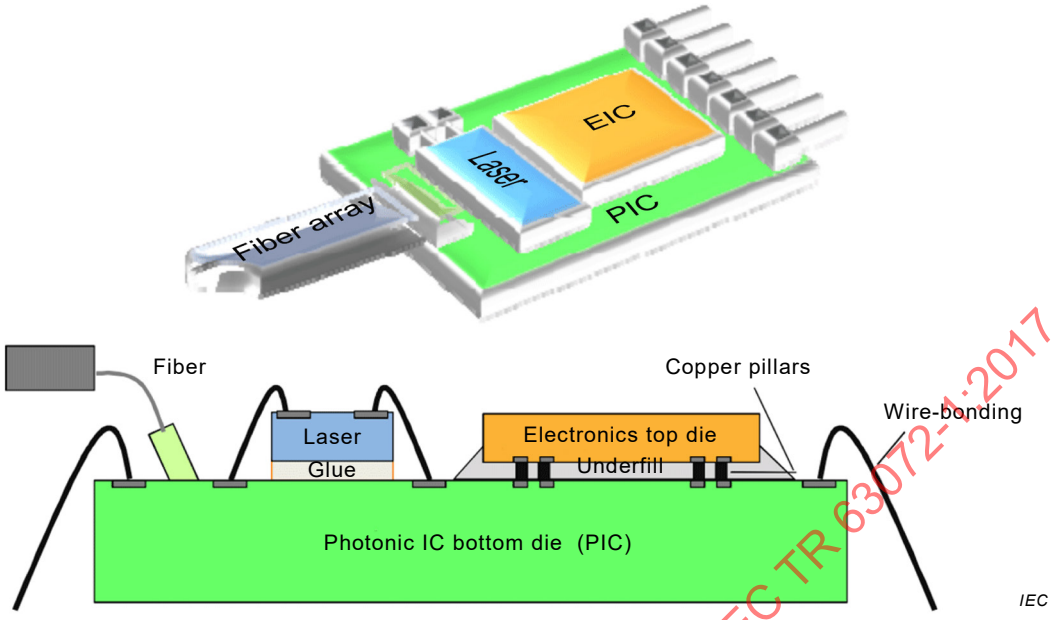
However, a number of more viable approaches to bonding III-V materials onto silicon wafers have emerged, including heterogeneous die-to-wafer bonding [14] through the use of adhesives such as BCB, molecular bonding processes, thermo-compression bonding [15], or hybrid Si evanescent devices [16].

Adhesive bonding materials such as BCB are poor thermal conductors, so devices based on adhesive bonding would typically need costly and power consumptive thermo-electric cooling (TEC) devices, such as Peltier coolers, to maintain critical thermal stability.

The University of California at Santa Barbara (UCSB) successfully demonstrated heterogeneous integration of InAlGaAs quantum well structured sources onto silicon waveguides using molecular bonding [17], [18].

Hybrid integration is a powerful approach that avoids many of the disadvantages of heterogeneous integration. Advances in the precision of pick and place assembly tools allows photonic chips to be positioned and bonded very rapidly on one another [19] (for example: accuracy ± 0,5 µm at 3 s, cycle-time < 15 s for the AMIRCA AFC Plus). Coupling efficiencies between the III-V waveguide and the waveguide on the silicon chip are less than that attained with heterogeneous integration, but values in excess of 50 % are possible. Advantages lie in the possibility to optimize the III-V chip for stand-alone operation, i.e. without the constraints of evanescent coupling, the highly efficient use of the costly III-V material. With suitable substrate preparation, the III-V chip can be put in direct thermal contact with the silicon.

Figure 8 shows an example of a hybrid 3D assembly for a quad optical transceiver whereby a separate laser source is glued onto the PIC and an electronic integrated circuit (EIC) is attached to the PIC using copper pillars.



SOURCE IEEE

Figure 8 – Schematic view of 3D assembly of PIC + EIC electro-optical assembly [6]

8.3 Vertical cavity surface emitting lasers (VCSELs)

The most popular choice of laser source from a cost and power consumption perspective is the vertical cavity surface emitting laser (VCSEL).

Unlike traditional edge-emitting semiconductor lasers, which emit parallel to the plane of the chip, VCSELs emit perpendicular to the top surface, which allows in-wafer testing prior to cleaving. VCSELs are today the most cost and power efficient and most widely used laser source for interconnects, due to their low threshold current, small size, direct modulation capabilities and their ability to be integrated in multi-component arrays. VCSELs are the dominant source for short reach optical communications based on 850 nm multimode transmission [20], [21]. However, VCSELs have also been produced for long-range single-mode interconnects in the 1 300 nm and 1 550 nm wavelength regions [22] by organisations such as Vertilas and V-I Systems in Germany, and RayCan in Korea. High-speed, long-wavelength VCSELs at 1 550 nm have been reported with data rates up to 35 Gb/s [23] or higher by using advanced modulation formats [24].

9 Optical receivers

Naturally, as with optical sources, optical receivers are indispensable in most PIC technologies.

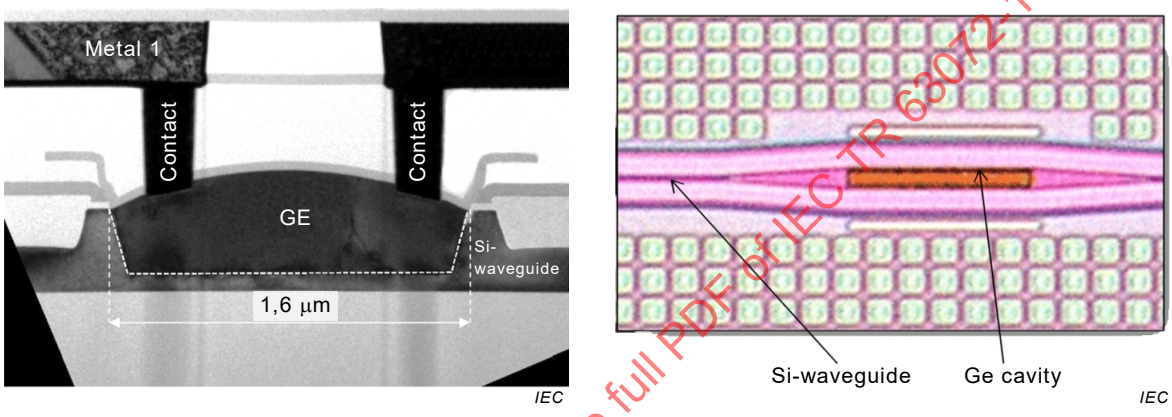
As with other direct bang-gap devices, the materials that form optical detectors are inherently highly absorptive and cannot be used to form the waveguides leading to the detector. Therefore, high speed PIC detector technology has gravitated towards the use of III-V or Germanium (IV) detectors bonded onto silicon waveguides, either through epitaxial growth or molecular bonding processes.

III-V materials such as GaAs are eminently suitable as optical detectors due to being direct bandgap materials; however, as described above, the integration of such devices onto silicon PICs is complicated, predominantly by the large lattice mismatch between the III-V and silicon material matrices, which becomes prohibitively expensive for high volume manufacturing and packaging applications.

Germanium (Ge), however, is a group IV material and, from an integration stand point, could be a more suitable alternative for light detection in the C-band, if it can be integrated monolithically onto silicon [25]. Although Ge, like silicon, is an indirect bandgap material, it has a direct bandgap energy of 0,8 eV, corresponding to a wavelength range from 1 100 nm to 1 600 nm. Under application of tensile strain, this bandgap energy can be further reduced to cover most of the C-band [26]. Several discrete Ge-on-Si photodetectors have been reported [27].

The most recent advances include several discrete Ge-on-Si photodetectors [28] and the successful integration of high speed silicon PIC modulators with Ge photodetectors on a single SOI platform [29].

Figure 9 shows an example of a Ge-on-Si photodetector formed by germanium selective epitaxy.



a) TEM cross-section of Germanium high speed photodetector

b) Top view of Germanium high speed photodetector

SOURCE IEEE

Figure 9 – Example of Ge-on-Si photodetector formed by germanium selective epitaxy [6]

10 Modulators

10.1 Overview

Modulators are integrated elements that allow electronic or optical signals to vary the amplitude of continuous wave light conveyed from an "upstream" source, such as a heterogeneously assembled laser or a coupling port to an external optical fibre.

Such "externally modulated systems" provide a higher performance alternative to directly modulated systems in which the optical sources themselves, typically semiconductor diode lasers, such as VCSELs, are directly driven by a varying electrical current. As of 2015, transceivers based on directly modulated VCSELs were generally less expensive and more energy efficient than PIC transceivers for on-off-keying modulation schemes up to 25 Gb/s.

However, with data communication protocols pushing the requirement for data rates beyond 50 Gb/s with low voltage, power consumption and footprint requirements before 2020, external modulation becomes a preferable option, especially when required for advanced modulation schemes such as 16-QAM.

10.2 Common modulator structures

In a Mach–Zehnder interferometer (MZI), the phase of light in the two arms is controlled either electro-optically (using the plasma dispersion effect) or thermo-optically (using the thermos-

optic effect). By inducing the appropriate relative phase change between light propagating along the two arms, MZIs can be designed to fully modulate the light through destructive interference.

Symmetric MZIs on which the length of both arms is the same result in wavelength and thermally insensitive operation.

Asymmetric MZIs on which the length of both arms is different are wavelength selective and thermally sensitive, with the operational wavelength and temperature being determined by the difference in effective path length between the two arms

In a micro-ring resonator (MRR), light propagating along a waveguide can be coupled to a small waveguide ring that is close enough to the waveguide to support evanescent coupling. Complete coupling of light from the waveguide into the MRR can only be achieved when the resonance condition is met, whereby the effective path length around the MRR is an integer multiple of the wavelength, as well as critical design parameters such as the gap between waveguide and MRR. The effective path length can be changed slightly by varying the refractive index on all or part of the MRR, so light can be modulated by moving the MRR into and out of a resonance condition. MRRs have a much smaller footprint than MZIs and a higher Q factor [30], [31]; however, they are more thermally sensitive than MZIs.

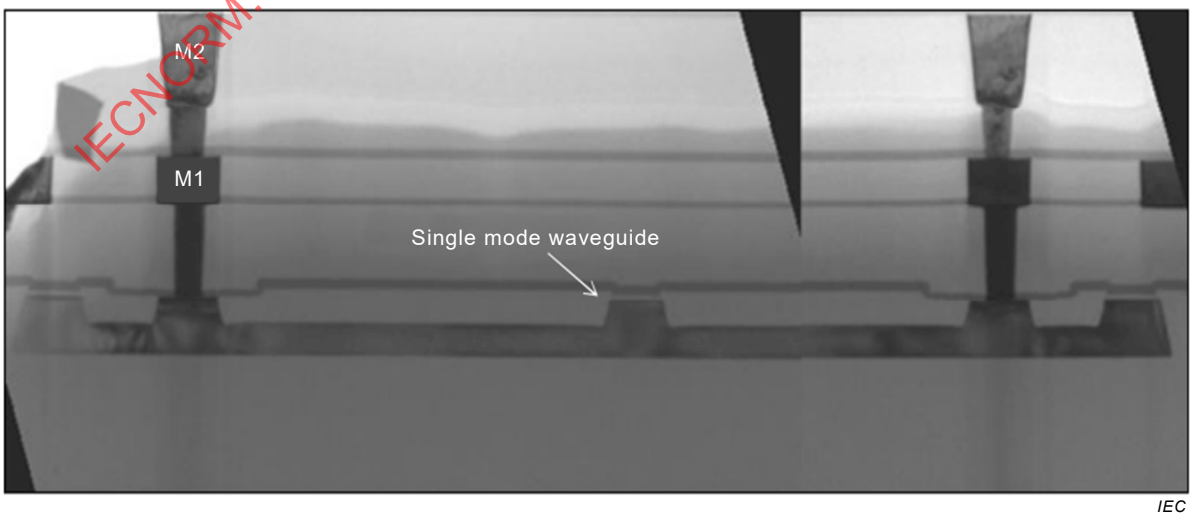
10.3 Plasma dispersion effect

State-of-the art silicon photonic modulators mainly rely on plasma dispersion effects on doped silicon or III/V-on-SOI.

Plasma dispersion modulation is derived from the change in refractive index induced by changes in space charge carrier density in positive intrinsic negative (PIN) diode or PN diode junctions and is a preferred modulation mechanism in silicon PICs, as it requires only two standard processes, doping and etching.

The two main approaches are: 1) charge injection, whereby space charges are added to the junction, through forward biasing across the junction; or 2) charge depletion, whereby space charge is removed, through a reverse bias of the junction, in order to induce the required refractive index change.

Figure 10 shows a cross-section of a high speed phase modulator (HSPM) based on a PN junction.



SOURCE IEEE

Figure 10 – High speed PN modulator [6]

Notable advances in plasma dispersion based modulation are reported in [32], [33], [34], [35], [36], [37], [38], [39]. More complex junction structures, such as PIPIN junctions, have also been demonstrated with modulation speeds of 40 Gb/s [40].

As of 2015, MZIs have emerged as the more practical choice of plasma dispersion modulator, as they offer high thermal insensitivity, robustness against fabrication variations, and modulation format support. Figure 11 shows the modulation scheme of a silicon PIC transceiver from the Photonics Electronics Technology Research Association (PETRA), which is based on a MZI with distributed MOSFET transistors along each arm providing an energy efficient push-pull modulation scheme.

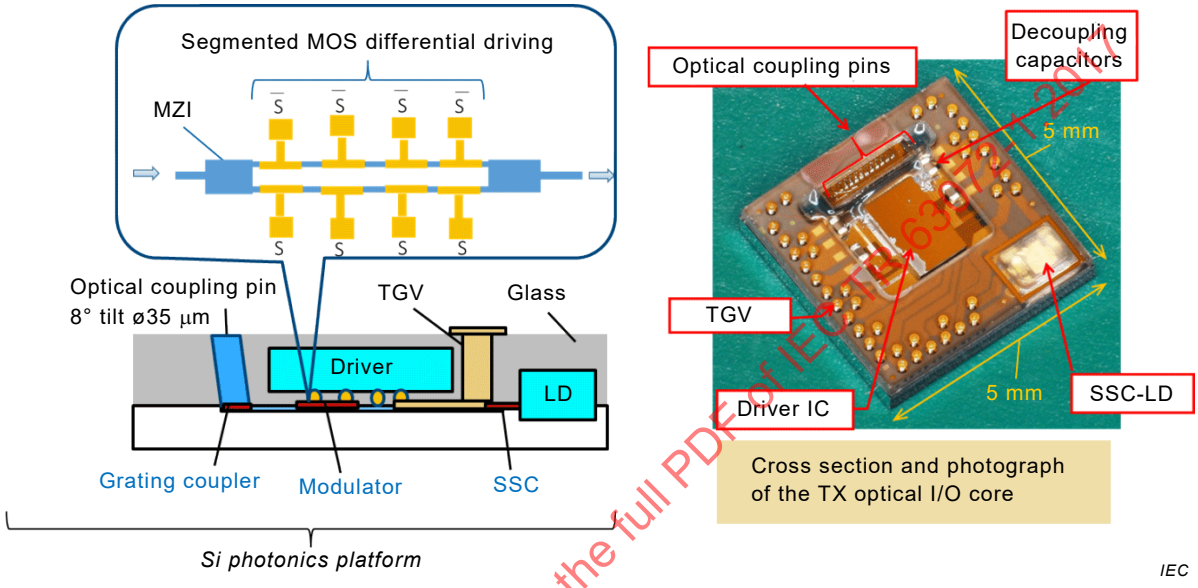


Figure 11 – PETRA optical I/O core chip modulation scheme

However, these structures typically need to be of the order of millimetres in size in order to achieve the relative phase change required for OOK modulation.

The size of modulation structures can, however, be reduced by deploying low dispersion slow light structures such as photonic crystal waveguides [41].

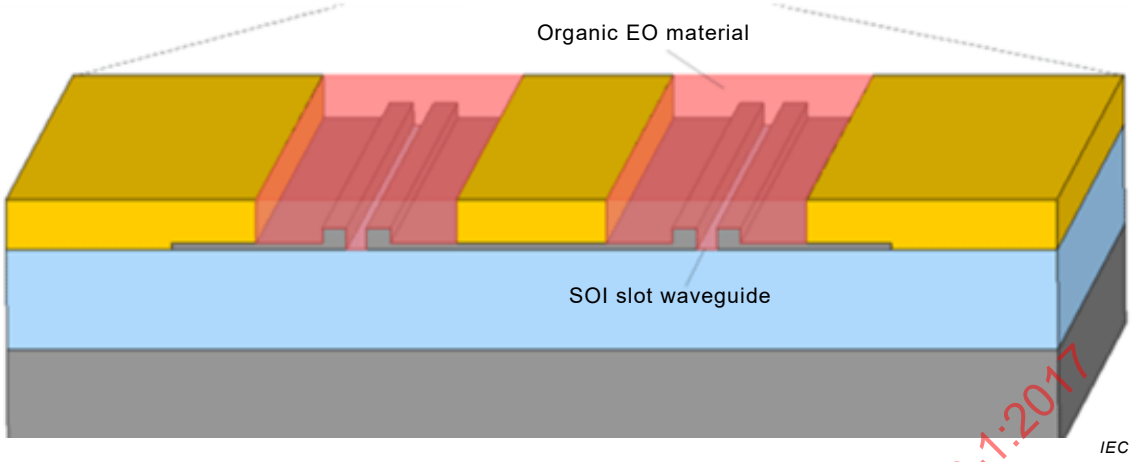
10.4 Plasmonics

Plasmonic effects have been the subject of research in Europe to exploit the presence of metallic traces for optical propagation and processing on PICs [42], [43]. Plasmonics relates to the propagation of collective electron oscillations across metallic traces, which is stimulated by light at a certain resonant frequency [44]. Therefore, metallic circuitry can also serve as plasmonic waveguides.

10.5 Silicon organic hybrid

The barrier of 100 GHz modulation frequency has been recently achieved by using silicon organic hybrid (SOH) technology [45]. SOH modulators exploit the ultrafast Pockels effect of high speed polymer materials deposited within a silicon photonic slot waveguide. An unprecedented 3 dB bandwidth of 100 GHz was achieved by employing a phase shifter of 500 µm length and 2 dB insertion losses, highlighting the impact of narrow slot waveguide configurations [46]. However, the overall performance of the SOH MZI modulator is degraded by the additional 9 dB losses due to the strip-to-slot and slot-to-strip tapering mode converters, which also result in the length of 2,6 mm.

Figure 12 is an illustration of silicon organic hybrid technology.



SOURCE Karlsruhe Institute of Technology

Figure 12 – Silicon organic hybrid

It has been forecast that plasmonics could overcome those trade-offs [47]. Recently, a group from ETHZ in Switzerland has introduced plasmonic organic hybrid (POH) devices and was able to demonstrate a 40 Gbit/s plasmonic phase modulator of 29 µm length [48] and Mach-Zehnder modulators (MZMs) operating at speed beyond 54 Gbit/s with a length of only 10 µm [49].

11 Switches

11.1 Overview

Switches are integrated elements that use phase shifting and interference processes to switch light from one or more input channels between multiple output channels. These processes are typically based on the same refractive index-changing mechanisms used for modulation as described above.

11.2 Mach-Zehnder interferometers (MZI)

The MZI is generally considered the preferred modulator structure compared to a MRR-based modulator, due to its thermal insensitivity, robustness to fabrication variations, and larger bandwidth.

Thermo-optic phase shifters for silicon on insulator switches have been employed successfully in 8 x 8 switch layouts with small footprints of 3,5 mm^2 x 2,4 mm^2 and also to larger circuits with up to 32 x 32 switching capabilities. The main drawback of thermo-optic actuation lies in its relatively low response time (~ 30 µs), which is not sufficient for fast packet-based traffic [50].

Electro-optical phase shifters exploiting the plasma-dispersion effect enable nanosecond response times. The main challenge when using free-carrier injection phase shifters is associated with their intrinsic losses, which set a bound to the minimum insertion loss and optical crosstalk that can be achieved from an elementary switching cell. 8 x 8 [51] and 4 x 4 (4 ns response) [52] switch layouts employing the carrier injection switch mechanism have been demonstrated.

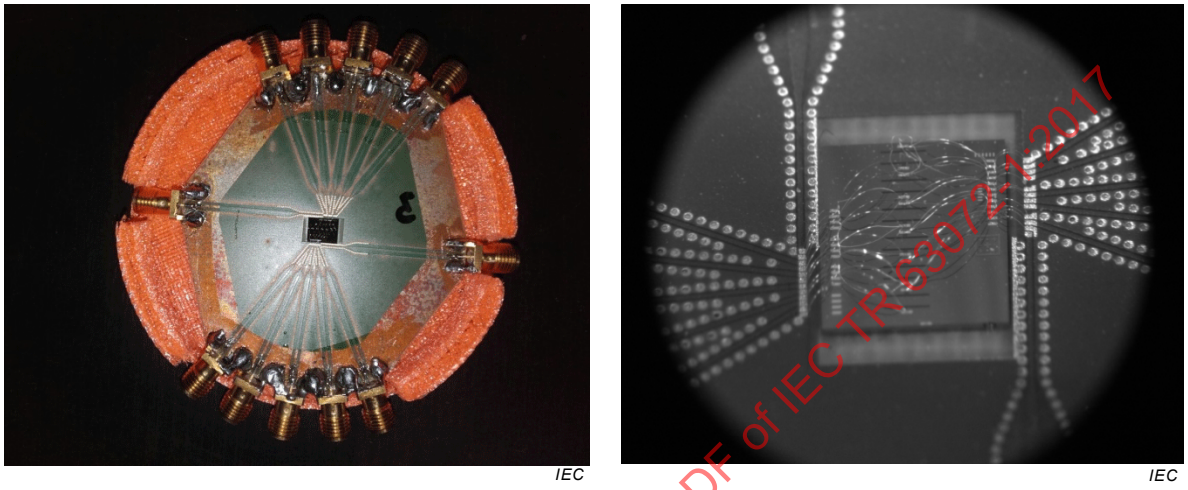
11.3 Micro-ring resonator (MRR)

In contrast to a symmetric MZI switch, the MRR switch like the MRR modulator is wavelength selective, the wavelength being determined by the resonance conditions of the MRR. Compared to MZIs, MRR-based switches are well-suited for chip-scale applications that

require very high bandwidth densities, but MRRs are dogged by higher sensitivity to temperature and fabrication tolerances. This can be mitigated to some degree by thermal stabilization and feed-back circuitry, but this increases cost and power consumption to the system.

11.4 Double-ring assisted MZI (DR-MZI)

The double-ring assisted MZI (DR-MZI) reported in [53] combines the merits of resonance enhancement in MRRs and the coherent interference in MZIs (see Figure 13).



IEC IEC

a) View of the packaged device **b) Magnified view of the device**

SOURCE AMS, Aristotle University of Thessaloniki

Figure 13 – 4 x 4 switching matrix PIC attached to PCB with wire bonds on the EU FP7 PhoxTroT project

12 3D integration

12.1 Optochip

The term "optochip" has emerged over the past few years to highlight the fact that photonic technology is slowly crossing the boundaries of a chip-set so far dominated by electronics. The idea behind this vision is to either deploy photonics as the switching fabric, vertically controlled by electronics and higher layer routing functionalities in high throughput routers, or integrate optical transceivers with supporting electronics and CMOS processors in next generation intra-chip interconnections, or both. Substantial advances in this area have been made by simultaneously progressing vertical integration techniques in the form of 3D integration (monolithic integration) and 3D stacking (hybrid integration), towards the vision of delivering multi-layer chip-sets accommodating both optics and electronics on the same socket [54].

12.2 Through-silicon-vias (TSVs)

Through-silicon-vias (TSV) may be used as "3D interconnects", leveraging all the advantages of heterogeneous integration, but on a common integration platform [55]. As previously described, electronics structures that reach down to the transistor polysilicon layer have been combined with optical waveguides to demonstrate active on-chip optical functionalities, such as modulation and switching [8], [9]. The 3D stacking approach enables heterogeneous integration of different technologies in order to combine multiple electronic and optical functions on a single chip [56]. 3D stacking photonic-electronic integration can be exploited with current state-of-the-art in III-V and SOI technologies in order to provide high performance optochips.

12.3 Hybrid integration process example

TSVs and hybrid integration have been combined also to embed the photonic layer into the last levels of metallization above the CMOS layer [57]. The process is described as follows:

- the CMOS wafer is processed up to the last metal layer, and the backside is thinned and fine polished to prime wafer surface quality;
- the photonic layer is then added through a low temperature wafer-to-wafer bonding process;
- in order to fabricate the TSVs forming the electrical connections between the CMOS layer and the photonic layers, deep silicon etching is performed down to the metal layer of the photonic layers;
- the TSV isolation and metallisation structures are deposited;
- the top metal layer, which connects the TSV with the IC and the passivation is deposited and structured;
- finally, the substrate wafer is removed in order to expose the photonic structures.

The key advantage of this approach is that the IC and the photonic processing steps are independent and can thus be separately optimised, and the packaging of such double-sided chips may be developed for other applications.

Optical TSVs in silicon [58], [59] and glass-based [60] interposers have also been demonstrated, whereby both optical and electronic signals can pass through the TSV.

Active photonic components have been integrated in a more complex chip in [55] with a VCSEL and a PD flip chip bonded on a 3D circuit.

Figure 14 shows a schematic view of the PhoxTroT 3D optochip concept, which is based on the assembly of discrete long wavelength single-mode VCSELs, photodiodes and high speed electronic drivers and receiver chips onto a silicon platform with integrated waveguides, grating couplers and TSVs.

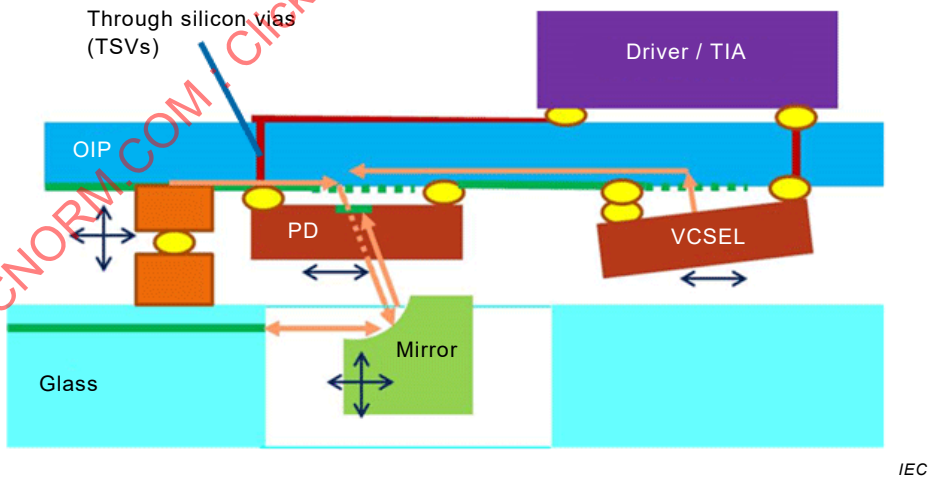


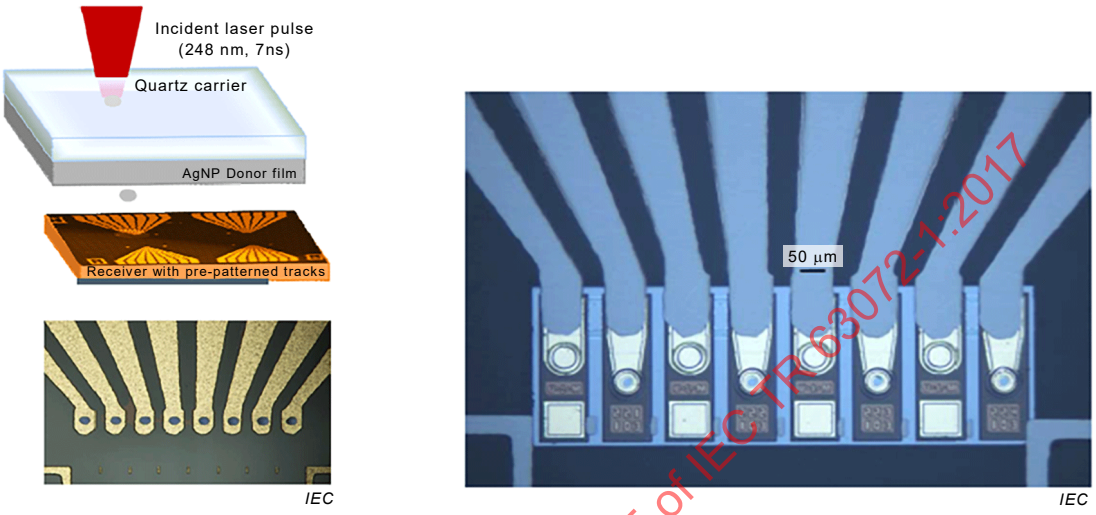
Figure 14 – EU FP7 project PhoxTroT 3D integrated optochip concept

12.4 Flip-chip bonding

Another method for optoelectronic assembly and vertical integration is flip-chip bonding, whereby contact bumps are required in order to connect the optoelectronic components with the substrate electrically, mechanically, and thermally. So far, two methods for flip-chip bonding of optical components on SOI substrates have been reported: soldering [61], [62] and thermo-compression bonding [63], [64]. Although this method imposes significant limitations in

terms of alignment accuracy, process complexity and mass production capabilities, it remains a promising assembly method for research purposes or small scale customized solutions.

More accurate methods of flip-chip assembly have been reported based on micro-bumps, which are defined through laser induced forward transfer (LIFT) of metal inks [65] to [67]. The principle of LIFT is schematically depicted in Figure 15.



a) LIFT principle (top) with optical micrograph of LIFTed AgNP ink microbumps (bottom)

b) VCSEL array after flip-chip bonding to microbumped substrate

SOURCE INTEC and Ghent University

Figure 15 – LIFT principle

12.5 State of the art in 3D research and development

IBM has dominated optochip research and development with the demonstration of two generations of the optobus program, achieving initially a total throughput of 160 Gbps (16 x 10 Gb/s) [68] and, more recently, 300 Gb/s (24 x 12,5 Gb/s) [69], consuming 8,2 mW/Gb/s. A newer approach was presented in [70], where 4 x 10 Gb/s transceivers were flip-chip bonded on a glass-formed PCB with 592 mW power consumption. Straight parallel polymer waveguides were fabricated with "waveguide-in-copper" technology in [71] with 4 x 10 Gbps transceivers flip chip bonded with ceramic ball grid arrays on the PCB as well. Optochips that operate with VCSEL in the 1 300 nm region for easier coupling to the waveguides due to smaller beam divergence were demonstrated in [72], with 4 x 10 Gb/s channels transmitted error free to the corresponding receivers. All these optochip developments have, however, targeted solely transmission/reception functionalities without encompassing any routing capabilities.

13 Commercial state of the art

13.1 Overview

As of 2016, a number of PIC transceiver technologies, based on CMOS platforms have entered the market, targeting optical interconnects for intra-data centre communication.

13.2 Luxtera

In 2007, Luxtera demonstrated a fully integrated, four channel, DWDM transceiver using interleaved optical multiplexers/demultiplexers, achieving an aggregate data rate of 40 Gb/s over a single fibre at a bit error ratio (BER) < 10^{-12} [73].

In 2008, the first ever demonstration of a fully integrated and programmable 40 Gb/s optical data communication system on a single SOI chip [74] was reported. The die included high speed MZI modulators, low-loss waveguides, high efficiency grating couplers, tuneable WDM multiplexers and demultiplexers, and monolithically integrated Ge-PIN waveguide photodetectors. The electronic receiver circuitry also includes high-speed transimpedance amplifiers and limiting amplifiers.

In September 2012, Luxtera reported [75] a 4 x 28 Gb/s transceiver module based on the same technology platform, which introduced several optimizations to reduce the transmitter footprint, with very good performance. It has to be noted that all process steps were performed with standard semiconductor fabrication manufacturing tools. The process development followed a methodology to ensure a capable process with proper assurances for process latitude and process monitoring. Within this process, particular emphasis was put on the development of a photonic device library including waveguides, optical I/Os, modulators and detectors. These elements were designed and optimized for minimum coupling loss to standard SM fibre of less than 0,8 dB [76].

The optical interface was a vertical grating coupler, which has the benefit of allowing the optical interface to be effectively be placed anywhere on the chip surface, thus allowing an increased density of optical interfaces and freeing the chip edge, which can be used for electrical signal pads. Surface coupling also enables wafer scale testing, providing valuable information that permits removal of non-functional dies before costly packaging processes. Another major cost advantage is the elimination of end face polishing.

13.3 Intel

Intel is also actively engaged in the development of PICs for optical interconnects. In July 2010, Intel announced an integrated silicon photonic transmitter capable of sending data at 50 Gb/s across an optical fibre to an integrated silicon photonic receiver chip, which converts the optical data back into electrical signals. The prototype incorporated several discrete technologies that Intel invented and combined into one package. These included a hybrid silicon/indium phosphide laser, a silicon modulator operating at 40 Gb/s, and a germanium detector, also operating at 40 Gb/s. These elements were brought together into a four-channel WDM link (1 351 nm, 1 331 nm, 1 311 nm and 1 291 nm), with each channel operating at 12,5 Gb/s, for a total bandwidth of 50 Gb/s. A multiplexer was then used to combine the optical channels and launch them into a fibre via an on-chip fibre coupler. A low-loss polarization-independent mode converter for coupling standard single-mode fibre to the silicon was used. For a micrometre-sized silicon waveguide, a coupling loss of 1 dB to 1,5 dB/facet has been measured as reported by Barkai [77].

On the receiver chip, optical signals received and separated by a 4-channel demultiplexer were then directed into four integrated germanium photodetectors. In January 2013, Intel and Facebook began collaboration on a new disaggregated, rack-scale server architecture based on the technology discussed above as part of the OpenCompute project [78].

13.4 Mellanox

Kotura, a PIC design and development house, acquired by Mellanox Technologies in the second half of 2013, is another key player in PIC-based transceiver fabrication. The PIC transceiver developed by Kotura comprises a separate transmitter PIC and receiver PIC as it is easier to package each as a transmitter optical sub-assembly (TOSA) and receiver optical sub-assembly (ROSA). The silicon PIC transmitter chip includes an InP platform incorporating an array of four lasers, which is flip-chipped onto the silicon PIC. Each laser comprises an InP gain chip connected to a resonant cavity, one end of which is located within the InP chip and the other end of which in the silicon PIC. The transmitter also includes a grating coupler tuned to each laser's wavelength, four modulators, and a WDM multiplexer to combine the four wavelengths before transmission out on the fibre. The receiver silicon PIC incorporates a four-channel demultiplexer with each demultiplexed channel passed to a Ge-PD. The device is similar to Luxtera's 100 Gb/s QSFP, which is described in Figure 7 and targets the same

switch applications in the data centre, but with the difference that Kotura is able to do wavelength-division multiplexing (WDM) on chip.

13.5 Oracle

Oracle developed and demonstrated a fully integrated silicon PIC transceiver in June 2012 [79], which used MRR modulators, operating at data rates of 25 Gb/s with a bit error rate of 10^{-12}. In addition to packaged modules, there have been efforts to produce highly integrated chip-like, multi-Gb/s/channel optical transmitters and receivers [80].

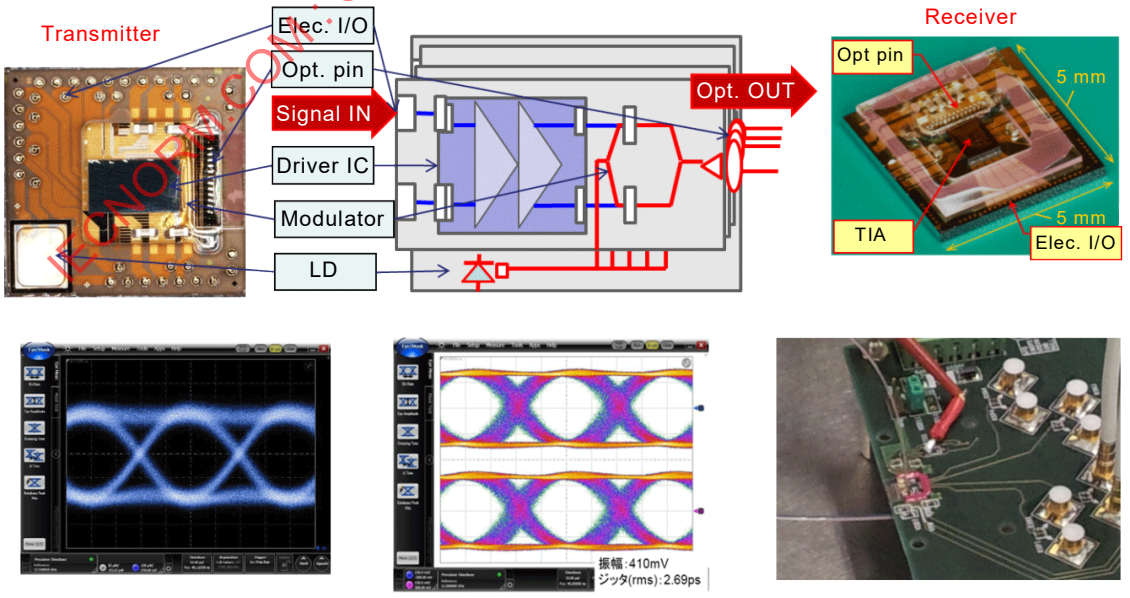
13.6 IBM

In 2012, IBM reported a 24 TX + 24 RX transceiver underpinned by a "holey" CMOS IC. The key component was the "holey" optochip, a single-chip CMOS IC fabricated in IBM 90-nm technology with 24 transmitter circuits plus 24 receiver circuits and incorporating 2 x 12 VCSEL and photodiode arrays. The optochip is then flip-chip soldered to a high-speed, high-density organic carrier, which is further soldered to a pluggable pin grid array (PGA) connector. The novel feature is the incorporation of 48 optical vias (holes) in the IC to enable optical access using industry-standard 850-nm optoelectronic arrays. All channels operated at 20 Gb/s (BER < 10^{-12}, 7,3 pJ/bit), achieving aggregate bidirectional bandwidth for parallel transceivers of 0,48 Tb/s [81].

13.7 Photonics Electronics Technology Research Association (PETRA)

PETRA is an incorporated technology research association in Japan, established on August 24, 2009. The organization is approved by METI (Ministry of Economy, Trade and Industry) under Japanese Act on an Incorporated Research and Development Partnership.

In 2015, PETRA developed a chip scale parallel optical transceiver capable of supporting data rates of 25 Gb/s per channel with a power consumption of 5 mW/Gbps. The PETRA silicon PIC "optical I/O core" transceiver was developed to target high volume, low-cost, short reach next-generation interconnections for IT systems and high-performance computers. The first variant of the optical I/O core contains a multimode optical interface, though variants with singlemode interfaces are planned. PETRA demonstrated 25-Gb/s per channel error-free operation over a 300-m MMF link in the O band as shown in Figure 16 [82] to [84].



Wave form of optical output at 25 Gbps

Electrical output in receiver

Evaluation board

IEC

Figure 16 – PETRA optical I/O core performance at 25 Gb/s

14 PIC coupling interfaces

14.1 Overview

In order to maximize the bandwidth density and design flexibility of PICs, vertical integration of electronic layers and photonics layers is strongly preferred. Numerous studies on optical interfaces have shown that optical signals can be coupled efficiently between PIC embedded optical waveguides on large-scale integration (LSI) chips and optical components outside a chip, such as optical fibres [85].

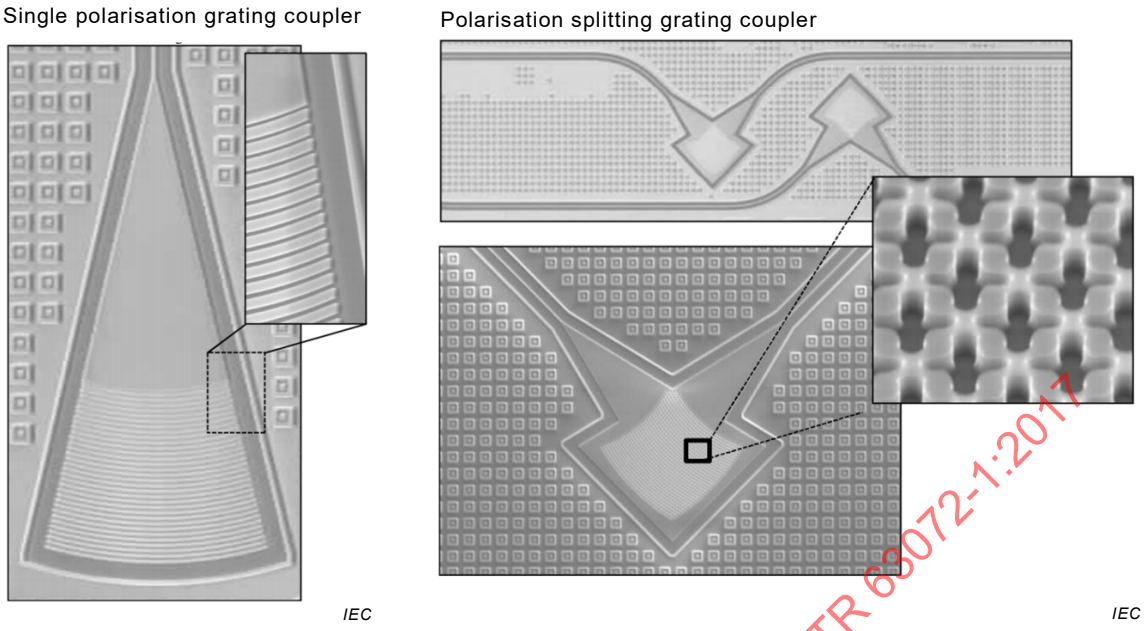
14.2 Grating coupler

Grating couplers were invented in the 1970's as a method of coupling free space laser light into glass films [86]. Grating couplers that can direct light waves irradiated perpendicular or nearly perpendicular to the surface of PICs have been widely studied [87] to [89]. The grating coupler is essentially a Bragg grating optimized to diffract light from a free space source into a dielectric waveguide. The coupling efficiency is determined by two factors:

- the directionality (D) defined as the ratio of the optical power diffracted toward the optical fibre to the total diffracted power;
- the mismatch between the diffracted field profile and the Gaussian mode of the optical fibre, which results in additional loss.

The diffracted filed profile originating from a uniform grating can be considered to be exponential. Thus, for a field mode diameter of 10,4 µm (value of SMF at 1,55 µm), the excess loss due to mode profile mismatch is 1 dB.

Figure 17 shows two common types of vertical grating coupler. Figure 17a) shows a single polarization grating coupler (SPGC) designed to couple light of one linear polarization to and from a waveguide in the PIC. SPGCs are typically used to transmit light from the PIC into an external single mode optical fibre in physical contact with the PIC surface. Figure 17b) shows a polarization splitting grating coupler (PSGC) designed to split the light incident on the PIC into two orthogonal linear polarizations, which are conveyed along two separate corresponding waveguides in the PIC. PSGCs remove any requirement on the input fibre to confine all light to one linear polarization and subsequently to orient the fibre to align the polarization axes of fibre and PIC waveguide. PSGCs are typically used to receive light from a single mode fibre and pass it to a photodetector on the PIC.



a) Single polarization grating coupler **b) Polarization splitting grating coupler**

SOURCE IEEE

Figure 17 – Examples of vertical grating couplers [6]

Since the coupling efficiency relies on diffraction properties of the grating structure used to couple light between an optical fibre and the silicon WG circuit, the coupling efficiency is inherently wavelength dependent, and the optical bandwidth, that is the wavelength range over which light can be coupled within a margin of 1 dB, is typically of the order of 35 nm [90].

Advanced CMOS technologies usually require bulk substrates or SOI substrates with thin SOI and buried oxide (BOX) [7]. The BOX thickness shall be optimized in order to minimize the insertion loss of grating coupler, used to couple the light in and out of optical fibres, in the targeted wavelength ranges, while ensuring a proper light confinement for low-loss propagation in waveguides. State-of-the-art coupling efficiencies are obtained for grating couplers, which are critical devices for silicon photonics since they allow the in and out coupling of external signal into the PIC. Median values of 2,15 dB (1 310 nm design), 1,5 dB (1 490 nm design) and 1,9 dB (1 550 nm design) for SPGC insertion loss are measured through the dielectric stack used for interconnect level [7]. More recently, an improved design of the grating couplers has shown that the efficiency of the fabricated coupler can be enhanced by a backside metal mirror and reaches –2,4 dB for both polarizations at 1 552 nm with an extinction ratio > 25 dB in a wide wavelength range [91].

Figure 18 shows the coupling efficiency of a single polarization grating coupler (SPGC) at 1 310 nm and 1 490 nm.

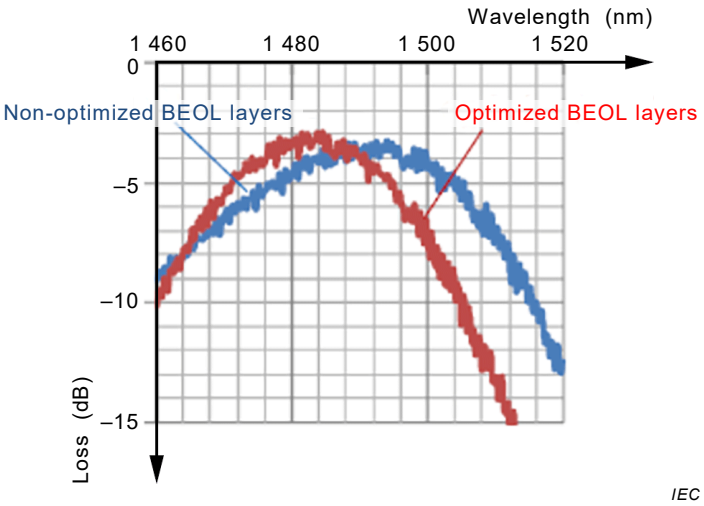
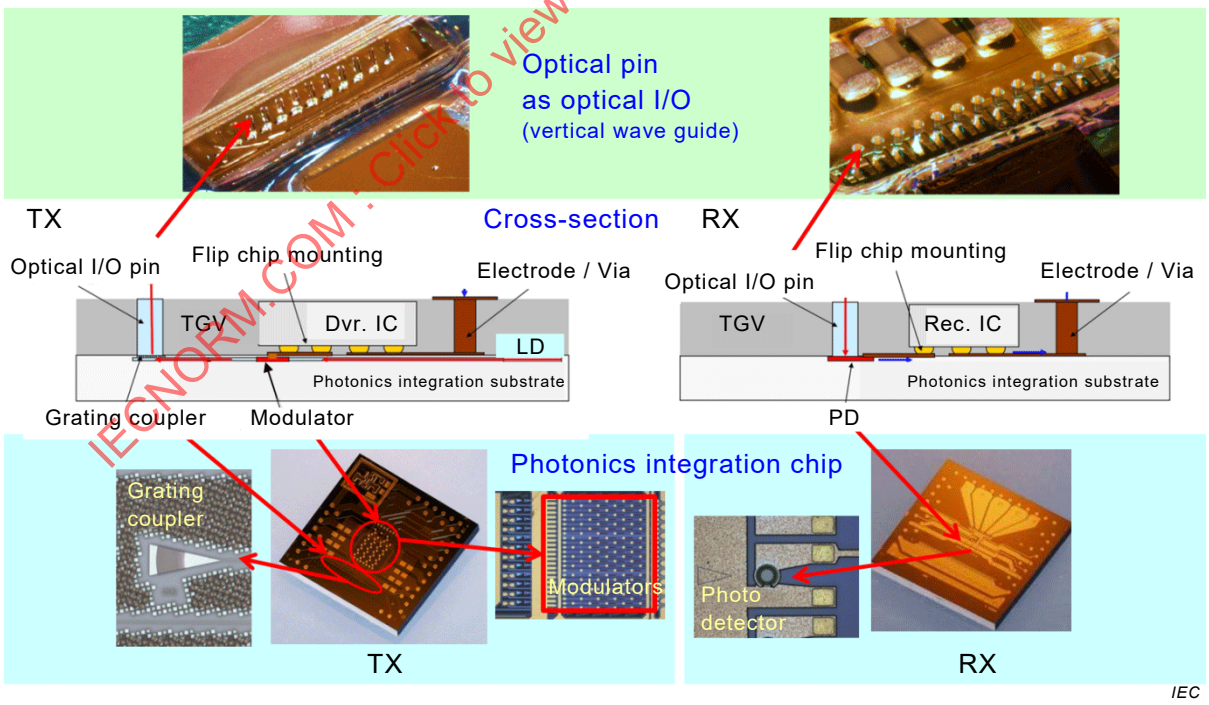


Figure 18 – Coupling efficiency of single polarization grating coupler (SPGC) at 1 310 nm and 1 490 nm [91]

In 2016, PETRA developed the first prototypes of a silicon PIC transceiver called the "optical I/O core chip", which used two kinds of vertical coupling interface for its transmitter and receiver sections (see Figure 19). A glass plate was mounted on the PIC, which provided both a protective barrier and a versatile optical coupling interface. On its transmitter section, a vertical grating coupler was used to direct light out of the silicon PIC through a special cylindrical through glass via (TGV) up to the top surface of the glass plate, which comprised the optical coupling interface. On the receive section, light was conveyed from the optical coupling interface through a TGV directly to a photodiode in the PIC.



SOURCE PETRA

Figure 19 – Composite coupling interfaces on PETRA optical I/O core

In 2015, University of British Columbia demonstrated the integration of VCSELs onto a silicon photonics chip using flip-chip bonding technique, with a bidirectional vertical coupled coupler [92].

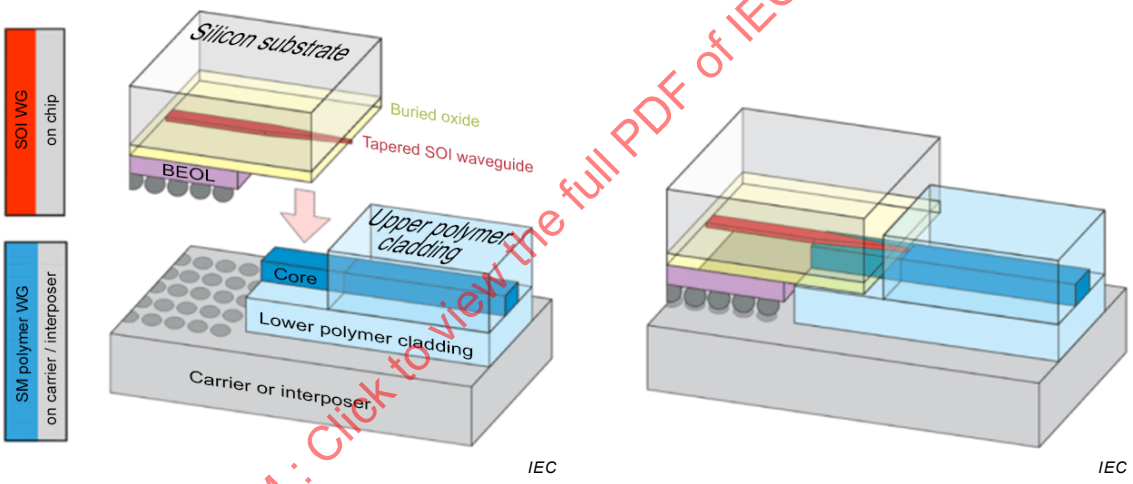
14.3 Adiabatic coupling

In 2013, IBM proposed an evanescent photonic chip optical coupling method based on flip-chip bonding on polymer waveguides [93], [94] to achieve low profile and pluggable coupling of a silicon photonics PIC. This concept relies on

- evanescent or adiabatic coupling from silicon waveguide to a polymer waveguide,
- passive positioning of both types of waveguide, using self-alignment, and
- passive positioning of the polymer waveguide into a MT-like ferrule.

This scheme uses the transition from a Si tapered waveguide to the polymer waveguide and required ~1,5 mm long tapers for a low loss coupling to occur from the Si to the polymer. This means that a large proportion of the PIC will be dedicated to the coupling region.

Figure 20 shows the assembly of a silicon photonics chip and a planar polymer waveguide in an adiabatic coupling configuration.



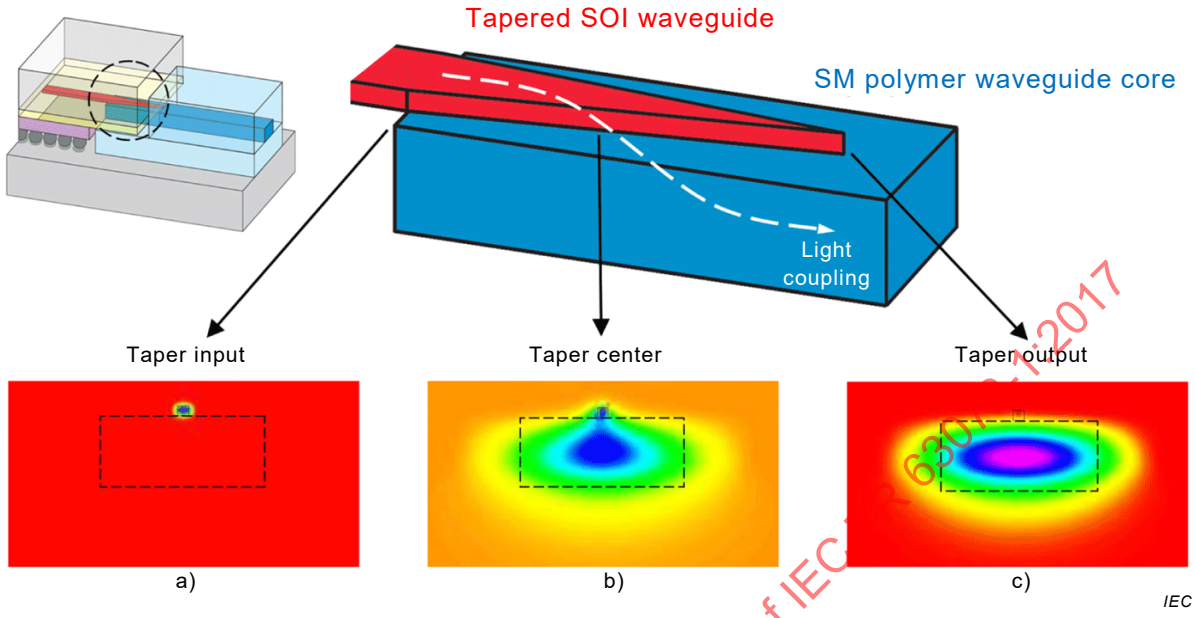
a) Locally tapered and un-cladded SOI waveguide on Si chip brought into physical contact with locally un-cladded SM polymer waveguide on carrier or interposer

b) Situation after assembly

SOURCE IBM Research – Zuerich [95]

Figure 20 – Assembly for adiabatic optical coupling between Si photonics chip and SM polymer waveguide

Figure 21 shows a schematic view of an adiabatic coupling scheme.

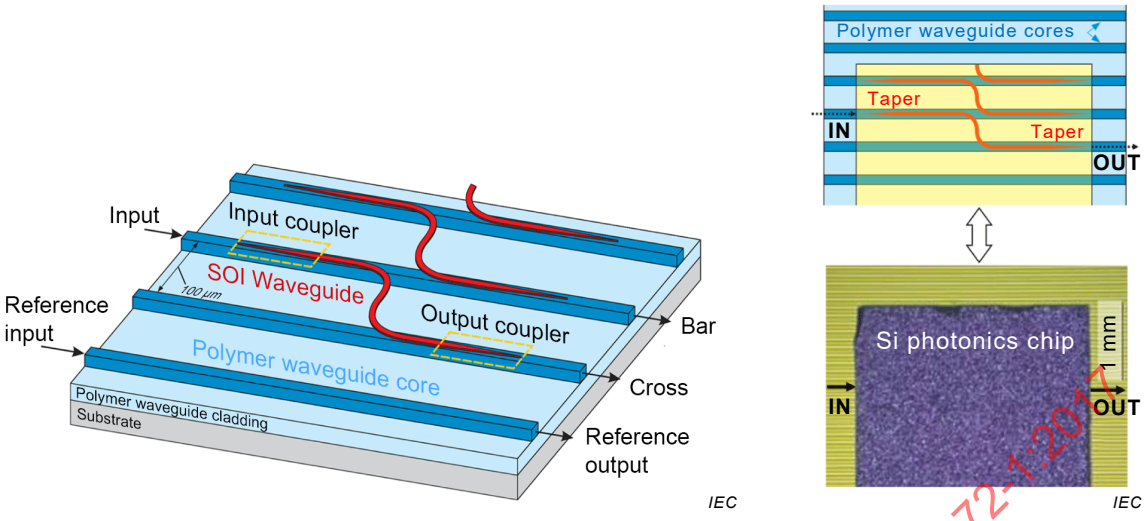


SOURCE IBM Research – Zuerich [95]

Figure 21 – Flip-chipped silicon photonic chip onto polymer waveguide substrate using adiabatic coupling

This approach has several advantages, among which are enabling attachment with multi fibre-channels and low profile and compatibility with on board packaging and mass assembly.

Bidirectional optical coupling between SOI waveguides and single polymer waveguides has been achieved by positioning the cores of SOI and polymer waveguides in close proximity and tapering down the SOI waveguide gradually, so that the eigenmodes of the coupled system evolve adiabatically along the coupler (see Figure 22).



a) SOI and SM polymer waveguide layout

b) SI photonics chip flip-chip-bonded to an array of un-cladded SM polymer waveguides

SOURCE IBM Research – Zuerich [95]

NOTE 1 The schematic in Figure 22a) proves the concept of adiabatic optical coupling. To characterize the coupler performance, the optical transmission of the input-to-cross, input-to-bar, and reference path had to be measured.

NOTE 2 Figure 22b) is a microscopic top-view [95].

Figure 22 – Bidirectional optical coupling between SOI waveguides and single polymer waveguides

Adiabatic coupling interfaces between polymer core and silicon waveguide have been demonstrated, which show coupling losses of the order of 1 dB for ± 1 µm misalignment (in-plane, transversal to optical axis), and no significant coupling loss due to temperature change was observable. Single-mode polymer waveguides were fabricated using a low cost maskless and etchless process. The optical characterization showed a coupling loss of 0,8 dB to 1,1 dB and 0,8 dB to 1,3 dB in the 1 530 nm to 1 570 nm range for TE and TM polarizations, respectively.

14.4 Butt coupling

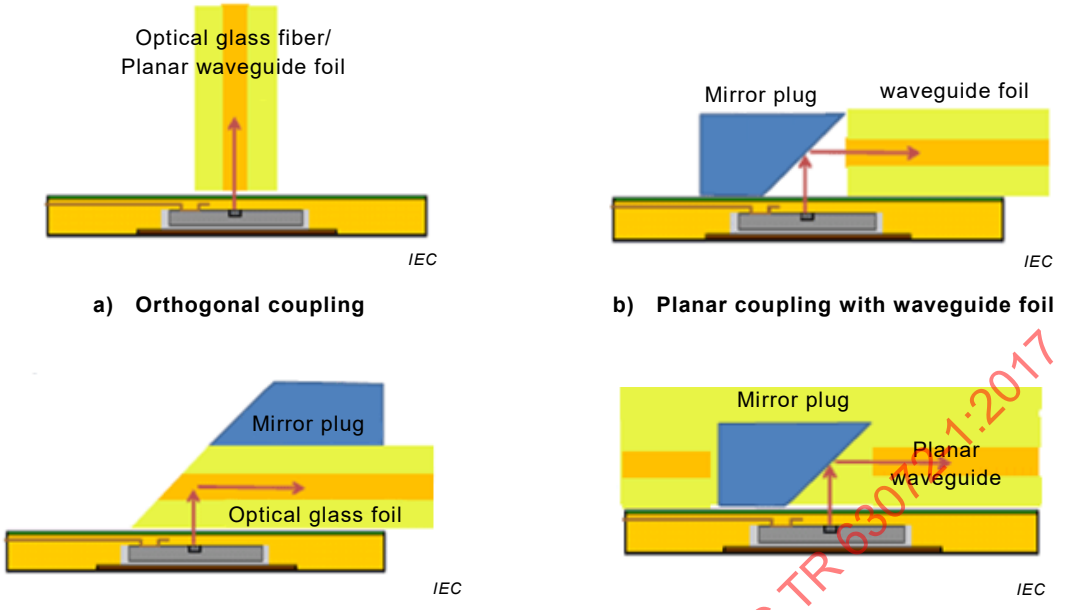
Fibre pigtailing ought to implement a reliable joint between a photonic device and a single fibre or a set/array of single-mode fibres. Pigtailing is a fundamental prerequisite for testing and application of photonic devices and is also the first step of packaged devices. Keeping in mind applications in telecom, a fibre-device joint should introduce as little as possible additional loss, low back-reflection, and low polarization dependence. Following the study of fibre couplers in previous clauses, we may distinguish between two kinds of pigtailing presently used in silicon photonics:

a) pigtails using lensed/tapered/high-NA fibres, typical spot diameter ~3 µm, horizontal coupling (example: Infinera);

b) pigtails using standard butt-fibres, spot diameter ~10 µm, horizontal and vertical coupling (examples: Kotura, Luxtera).

14.5 Orthogonal chip-to-fibre coupling

More recently, opto-electronic assembly processes have been developed by University of Ghent allowing embedded optical chips to be coupled orthogonally to waveguides or fibres [96], which offers a means of using robust surface grating couplers in low profile packages. Figure 23 shows different coupling scenarios based on embedding ultra-thin VCSEL and photodiode chips into thin polymer layers and coupling directly to planar polymer waveguides. Figure 24 shows an image of a mirror plug assembly, which also incorporates an optical fibre.

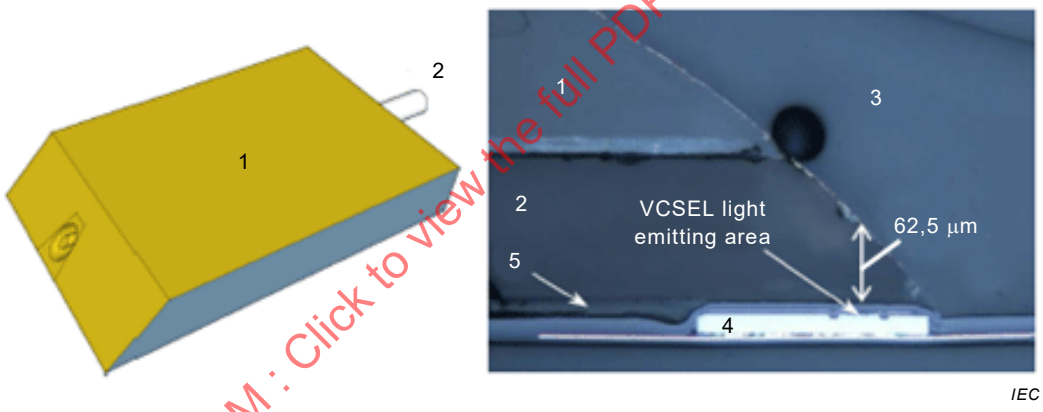


a) **Orthogonal coupling**

b) **Planar coupling with waveguide foil**

c) **Planar coupling with optical glass fibre**

d) **Planar coupling with a planar waveguide**



Key

1 with integrated silica fibre

2 with polished 45 degree end facet

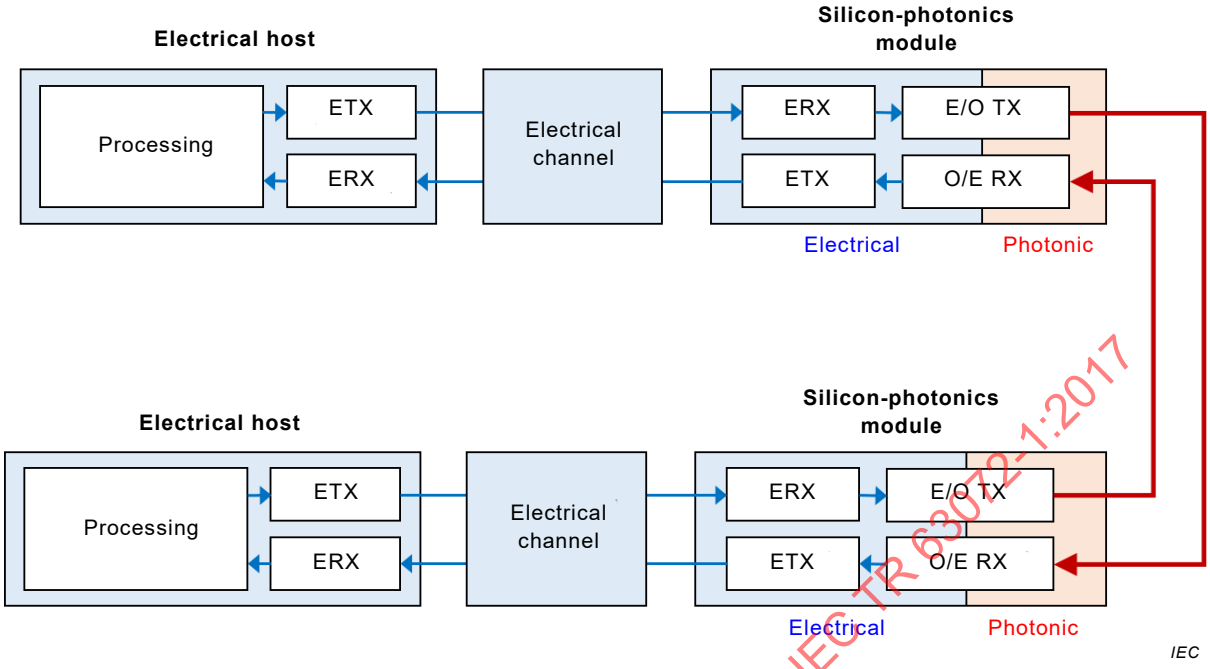
3 and 5 together with a cross-section of the UV-adhesive mounted mirror plug on top of embedded VCSEL chip

4 embedded VCSEL chip

Figure 23 – Design of the mirror plug assembly

15 Electrical interface

The electrical interface is responsible for the biasing and driving of the photonic components and their communication with the electrical environment in which the silicon photonics module operates. A typical framework is depicted in Figure 24. Electronic circuits are required to directly bias and drive the photonic components as an interface between the electrical and the optical domains. Moreover, several electrical functions are necessary to ensure proper communication of the silicon-photonics module with the host. Specifically, the electro-optical transmitter requires a dedicated electrical receiver to correctly receive the incoming data from the host, and the electro-optical receiver requires a dedicated electrical transmitter to send the data to the host. The E RX and E TX have to compensate the detrimental effect of the limited bandwidth of the electrical channel by implementing equalization.



SOURCE University of Pavia

Figure 24 – Typical operative framework of silicon-photonics modules

16 Packaging

Packaging of photonic devices has in general been a challenge over the years. A package assembly needs to fulfil a number of functions:

a) provide electrical and optical interfaces;

b) provide thermal interfaces;

c) protect internal devices from external influences such as humidity, effects from thermal excursions, contamination and mechanical forces [97].

Both assembly processes for photonic assemblies are important since they affect performance, reliability and cost.

It is important to develop standardized packaging platforms to accelerate PIC development and technology commercialisation.

17 Standardization roadmap

PICs are an emerging technology, which, as of 2015, had begun to be incorporated into commercial optical communication products. However, given its huge potential, PIC technology is expected to be subject to extensive research and development for many years to come.

As always, though standardization need not be a prerequisite to commercial deployment, if properly exercised, it will serve as a grounding and positive guiding force for emerging technologies.

It is, therefore, crucial that any PIC standardization activities proceed in a manner that does not in any way impede or constrain ongoing innovation.

The main purpose of early standardization should be to aid commercialisation of the technology by first creating competitive performance benchmarks, which provide realistic goals to those areas of mature PIC research hoping to commercialise the technologies.

The proposed standardization roadmap for PIC is shown in Figure 25.

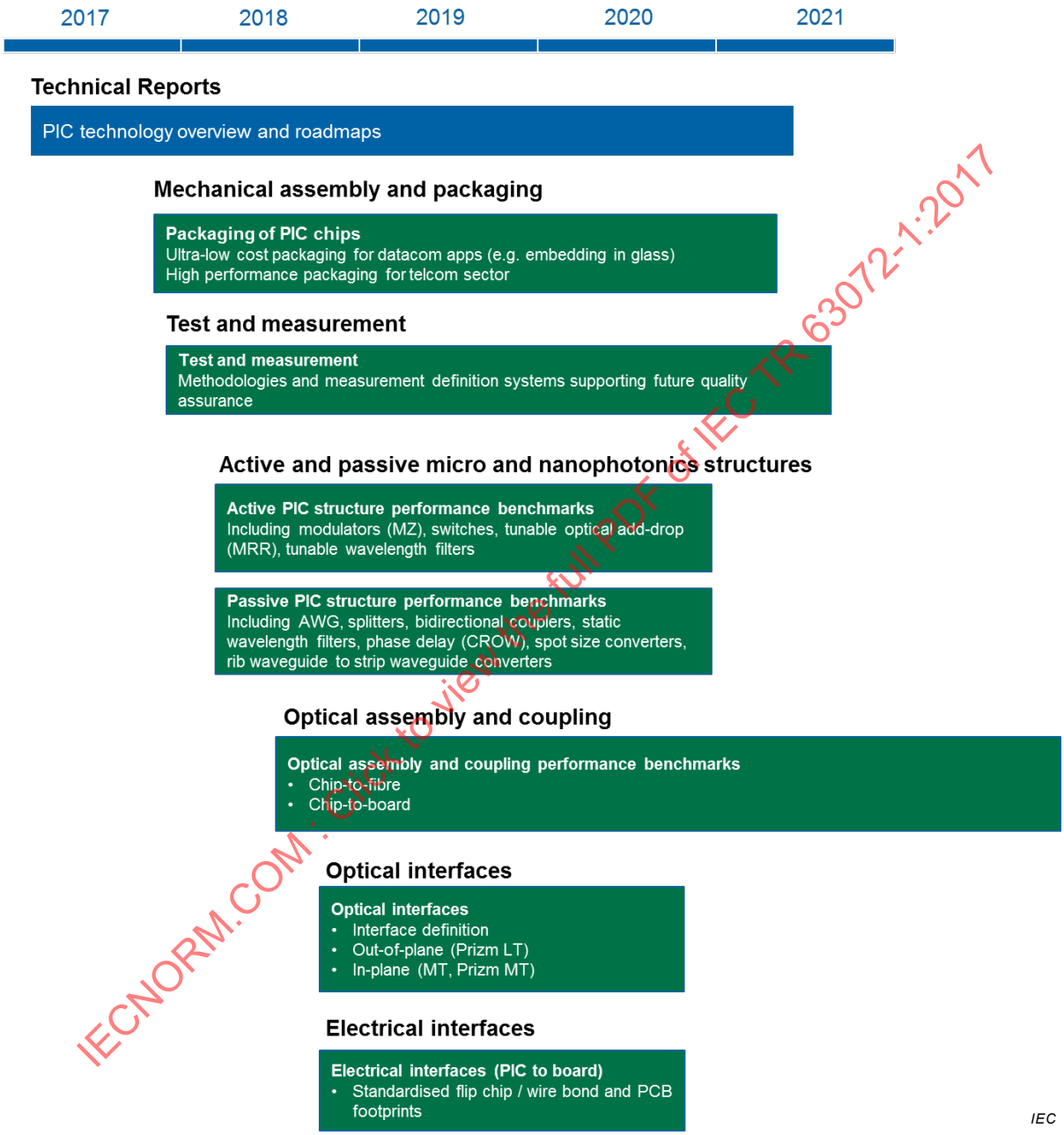


Figure 25 – PIC standardization roadmap